Paper

An impact of frequency on capacitances of partially-depleted SOI MOSFETs

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Abstract — A non-quasi-static model of partially-depleted SOI MOSFETs is presented. Phenomena, which are particularly responsible for dependence of device admittances on frequency are briefly described. Several C-V characteristics of the SOI MOSFET calculated for a wide range of frequencies, preliminary results of numerical analysis and of measurements and brief analysis of the results are presented. Methods of model improvement are proposed.

Keywords — SOI MOSFET, small-signal models, non-quasi-static analysis, admittances.

1. Introduction

One of the main advantages of silicon-on-insulator (SOI) CMOS circuits is their speed, which results mainly from the reduced parasitic capacitances of SOI MOSFETs. However the C-V characteristics of partially-depleted (PD) SOI MOSFETs exhibit a relevant dependence on frequency. This effect results from the floating-body phenomena, which are due to the fact, that thin active film of the PD SOI MOSFET is surrounded by dielectric layers and junctions. A detailed numerical analysis of the physical phenomena in the PD SOI MOSFETs for small-signal excitation consitions was presented in [1], where a new mixed quasi-static (QS) / non-quasi-static (NQS) scheme of transient phenomena treatment was used. The main conclusions resulting from this work confirm the above mentioned features of the PD SOI MOSFETs and their C-V characteristics.

The reliable models of the PD SOI MOSFETs admittances, which account for the floating-body phenomena may be useful for characterization and CAD purposes. However, analytical models of the PD SOI MOSFETs admittances derived so far are based primarily on the QS aproach [2, 3], which does not allow to obtain frequency dependence of device capacitances. Such analysis is possible using the NQS methods, but there are only very few models of this category [4]. Moreover they are represented in AC domain not by appropriate set of equations, but rather by equivalent circuits. Small-signal current equations and admittances result from these circuits. Thus it is very difficult to ensure consistency between DC models and their small-signal counterparts.

In this work some results of analysis of frequency effect upon C-V curves of PD SOI MOSFETs are presented. They were obtained using the recently derived NQS model of the PD SOI MOSFETs in the strong inversion range [5]. This model is formulated as a set of current equations in the complex numbers domain. In case of conduction currents their AC components were obtained through linearization of the appropriate DC currents expressions. In case of displacement currents they were obtained as derivatives of the appropriate charges. Thus the AC and DC models of the PD SOI MOSFETs are fully compatible.

2. Small-signal currents components in the PD SOI MOSFET

The general Eq. (1), which describes transistor behaviour in the AC domain represents obviously condition of balance of all currents flowing into the device:

$$i_s^* + i_{gf}^* + i_d^* + i_{gb}^* = 0\,. \tag{1}$$

All the components of formula (1) denote phasors (complex amplitudes of the small-signal components) of the source, front gate, drain and back gate currents, respectively. The Eq. (1) is linear in terms of v_{bs}^*, i.e. phasor of the time-dependent body-source voltage $v_{bs}(t)$. With the given v_{bs}^* AC components of all currents in the device may be determined. Then the small-signal admittances may be obtained using the following formula

$$Y_{xy} = G_{xy} + j\omega C_{xy} = \left.\frac{i_x^*}{v_y^*}\right|_{v_z^*=(0,0),\, z\neq y}\,. \tag{2}$$

Below these current components are briefly described.

3. AC components of gates currents

Small-signal currents flowing into both gates consist of intrinsic and extrinsic, parasitic components

$$i_{gf(b)}^* = i_{gf(b),i}^* + i_{gf(b)s,ex}^* + i_{gf(b)d,ex}^*\,. \tag{3}$$

Intrinsic components $i_{gf(b),i}^*$ result from charging/discharging of gates electrodes associated with the so-called „ideal" (intrinsic) MOSFET. They contain also currents $i_{sb,f(b),displ}^*$, $i_{db,f(b),displ}^*$, related to inner fringing field, which will be described in the next section. Extrinsic components $i_{gf(b)s,ex}^*$ and $i_{gf(b)d,ex}^*$ are related to overlap and outer fringing capacitances [6]. They are shown in Fig. 1.

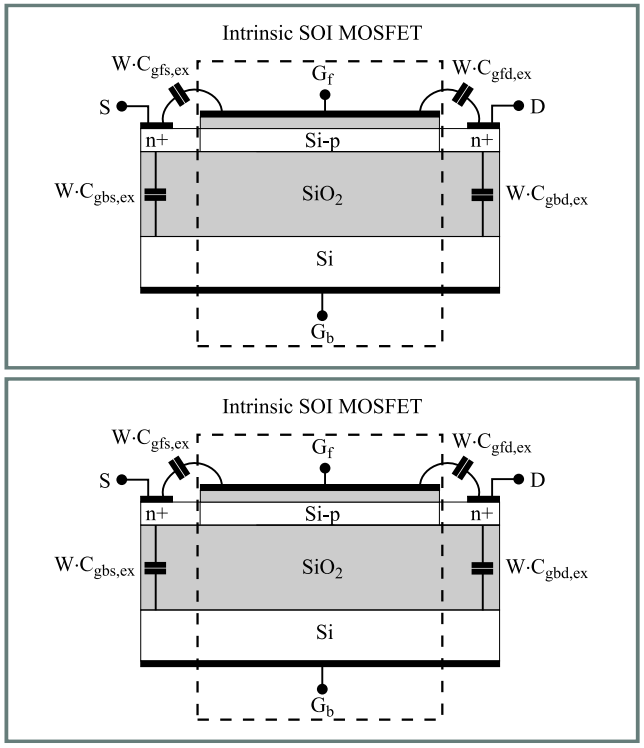


Fig. 1. Parasitic front/back gate-source/drain capacitances in PD SOI MOSFET.

These currents can be approximately considered as purely capacitative ones, because they depend only on voltages of the electrodes. They do not depend on spatial distribution of AC component of surface potential, so they do not exhibit additional phase shift relative to electrodes voltages.

4. AC components of source and drain currents

AC currents flowing into the source and drain are expressed as superpositions of several components, which are related to different phenomena at source and drain boundaries respectively.

$$i_s^* = i_{sb,diff+rec+displ}^* + i_{sb,f,displ}^* + i_{sb,b,displ}^* - i_{gfs,ex}^* + \\ - i_{gbs,ex}^* - i_{drift,f}^*(0) - i_{drift,b}^*(0)\,, \tag{4}$$

$$i_d^* = -i_{db,diff+gen+aval+displ}^* - i_{db,f,displ}^* - i_{db,b,displ}^* + \\ - i_{gfd,ex}^* - i_{gbd,ex}^* + i_{drift,f}^*(L) + i_{drift,b}^*(L)\,. \tag{5}$$

The variables in the above formulae have the following meaning:

$i_{drift,f(b)}^*(0)$, $i_{drift,f(b)}^*(L)$ – AC components of the channel drift currents at the front (back) Si-SiO_2 interfaces, which flow through the source (y = 0) or drain (y = L) contacts; they are determined by the approximate solution of current continuity equation; method of solution was adapted from [7] and generalized in order to account for body voltage variations; in the saturation range AC currents at the drain contact account for avalanche ionization in the „pinch-off" region;

$i_{sb,diff+rec+displ}^*$ – total AC current, which flows through the bulk part of the source-body junction, which consists of two conduction components: diffusion and recombination currents and of displacement current;

$i_{db,diff+gen+aval+displ}^*$ – total AC current, which flows through the bulk part of the drain-body junction, which consists of two conduction components: diffusion and recombination currents and of displacement current; conduc-

tion currents are multiplied by avalanche ionization in the depletion region of the junction;

$i^*_{sb,f(b),displ}$, $i^*_{db,f(b),displ}$ – displacement currents (mentioned in the previous section), which are related to the inner fringing fields between the source (drain) and front (back) gate; in the presente model they result from the modulation of the widths of the source (drain) controlled space-charge areas by the appropriate gate DC bias;

$i^*_{gf(b)s,ex}$, $i^*_{gf(b)d,ex}$ – displacement currents related to overlap and outer fringing capacitances (described in the previous section).

The AC components of drift, diffusion, generation/recombination and avalanche ionization currents are described by the NQS models, so they exhibit dependence on frequency. Thus the admittances of the PD SOI MOSFETs should also be frequency dependent. In the next section this effect will be briefly described and illustrated by simulated data. Also preliminary results of numerical analysis and of measurements will be presented.

5. Effect of frequency on selected C-V curves

C-V characteristics of the PD SOI MOSFET were calculated using the model presented in the previous sections. Parameters of this device are listed in Table 1.

In Fig. 2 $C_{gfs}(V_{GfS})$ characteristics obtained for a range of frequencies and for two drain-source voltages are shown. A strong influence of frequency on these curves is evident. The main feature of these data is decrease of the C_{gfs} value in the strong-inversion range, when frequency increases to hundreds of megahertz. This means, that at high frequency a phase shift between voltage and current AC components significantly changes. Due to the non-quasi-static behaviour gate capacitor properties are changed. More detailed analysis could be done using conductances behaviour at high frequencies. Another feature is that at the boundary between the subthreshold and saturation ranges a decrease of C_{gfs} below zero Farads can be observed. This effect is rather not induced by strong field effects, because it diminishes when drain voltage increases. This effect requires further investigation. One of the possible approaches could be improvement of small-signal model of drift current in high-frequencies range. It would require accounting for higher-order terms in solution of integral equation [7].

Figure 3 shows influence of frequency on C_{gfd} capacitances. Weaker dependence of C_{gfd} on frequency (than in case of C_{gfs}) is probably due to the fact that C_{gfd} increases in non-saturation range, when channel is shortly connected to the drain electrode.

Figure 4 shows very strong influence of frequency on C_{gfgb}, which can be observed particularly at the border between subthreshold and saturation ranges (like in case of $C_{gfs}(V_{GfS})$ data). At higher frequencies the influence of gate bias on the capacitance diminishes.

Figures 5 and 6 show influence of frequency on C_{ds} and C_{sd}

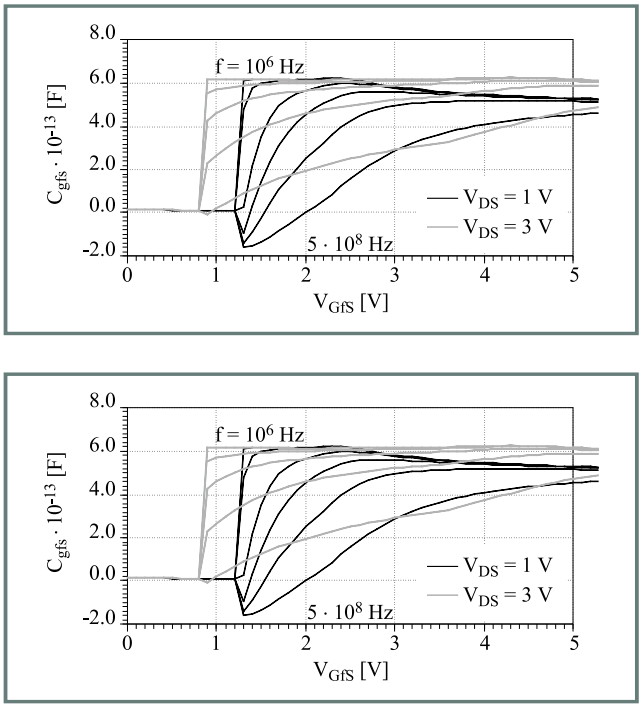


Fig. 2. Simulated $C_{gfs}(V_{GfS})$ characteristics of the PD SOI MOSFET ($V_{GbS} = 0$ V) for frequencies: 10^6, 10^7, $5 \cdot 10^7$, 10^8, $2 \cdot 10^8$, $5 \cdot 10^8$ Hz.

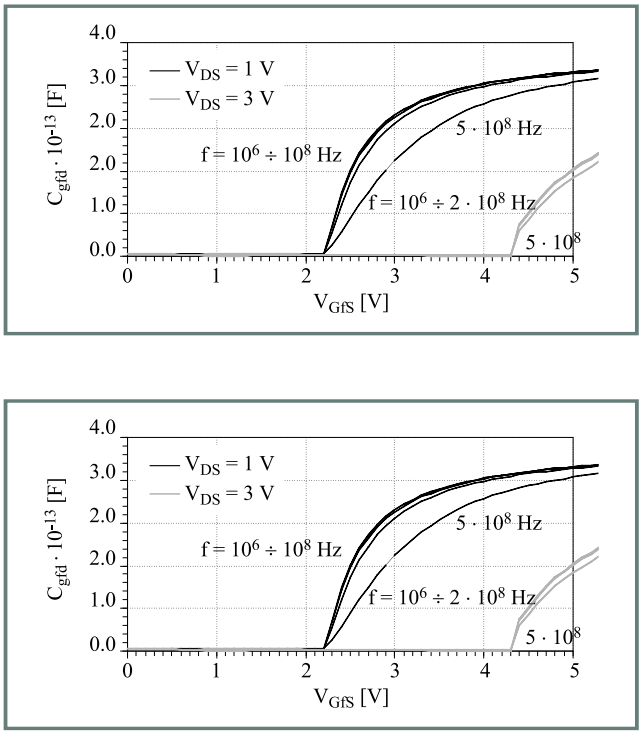


Fig. 3. Simulated $C_{gfd}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.

capacitances and non-symmetric (non-reciprocal) character of these curves. Very strong influence of frequency on C_{ds}

Table 1
Parameters of the simulated PD SOI MOSFET

Parameters	Value
Width (W)	100 µm
Length (L)	9.4 µm
Front gate oxide thickness (T_{Oxf})	32.8 nm
Back gate oxide thickness (T_{Oxb})	400 nm
Si film thickness (T_{Si})	150 nm
Doping conc. In the Si film (N_B)	9×10^{16} cm^{-3}
Fixed charge density at the front Si-SiO_2 interface (N_{ssf})	3×10^{10} cm^{-2}
Fixed charge density at the back Si-SiO_2 interface (N_{ssb})	10^{11} cm^{-2}
Mobility in the front channel (μ_f)	318 cm^2/Vs
Mobility in the back channel (μ_b)	318 cm^2/Vs
Recombination life-time in the body (τ_B)	10^{-6} s
Recombination/generation life-time in the junctions (τ_J)	10^{-7} s
Temperature	22° C

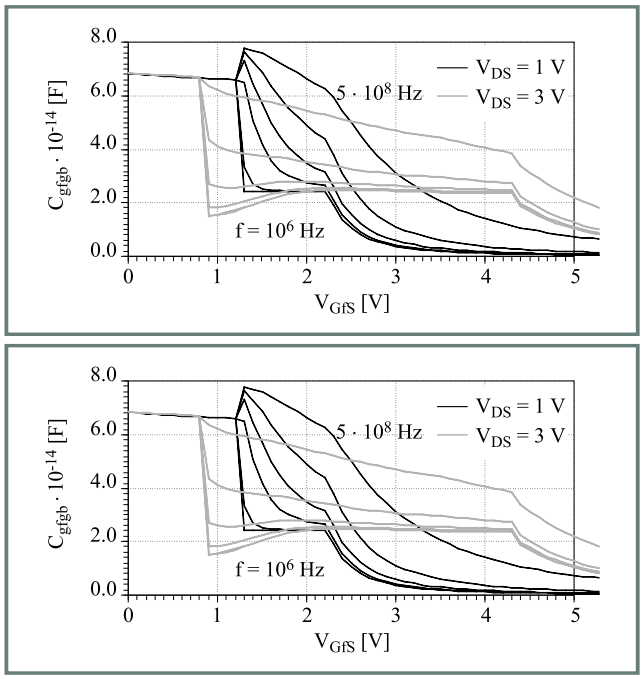
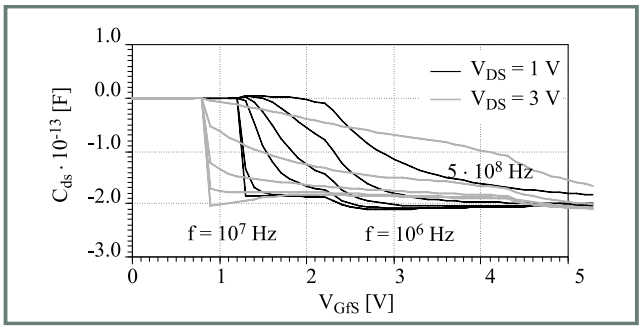


Fig. 4. Simulated $C_{gfgb}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.

can be observed in the saturation range, when the drain current flows through the „pinch-off" region, where avalanche multiplication dominates. Much more weak influence of frequency on C_{sd} (as compared to C_{ds}) can be observed. Then the channel is shortly connected to the source node. It is analogous to the C_{gfs}, C_{gfd} pair of capacitances, which were compared above.

6. Experimental and numerical data (preliminary results)

In order to support the need of non-quasi-static modelling of SOI MOSFETs preliminary measurements of the PD SOI MOSFETs capacitances were done using the HP5275A LCR-meter. Figure 7 shows two $C_{gfs}(V_{GfS})$ curves of the MOSFET (device parameters are in the figure caption) obtained for two frequencies of measurement signal: 10^5 Hz, 10^6 Hz. The results of the measurement are not clear. In this range of frequencies there is only a slight difference between both curves. It is in agreement with the results presented earlier, where the relevant variations of capacitances were observed at much higher frequencies. Thus using these experimental data it is difficult to make conclusions about the correctness of the model and about the



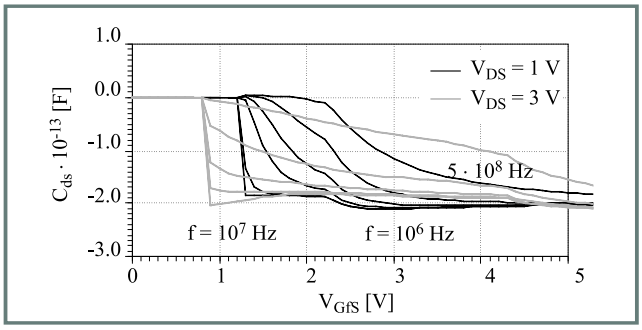


Fig. 5. Simulated $C_{ds}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.

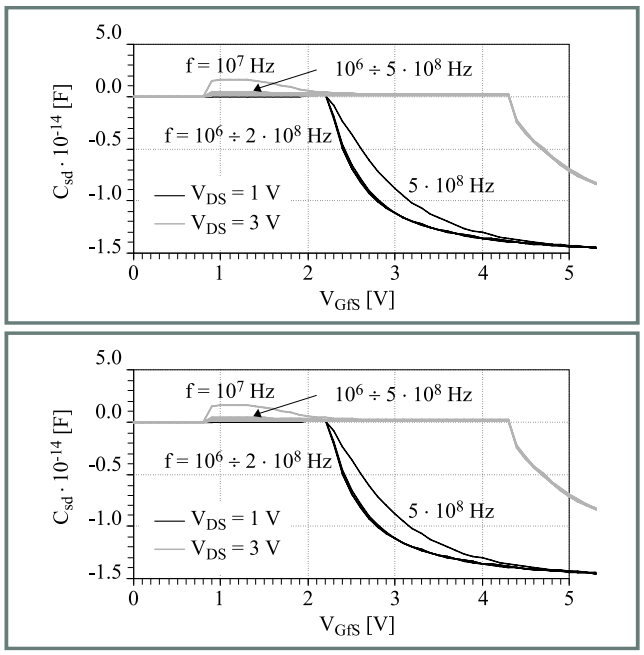


Fig. 6. Simulated $C_{sd}(V_{GfS})$ characteristics of the PD SOI MOSFET for the range of frequencies.

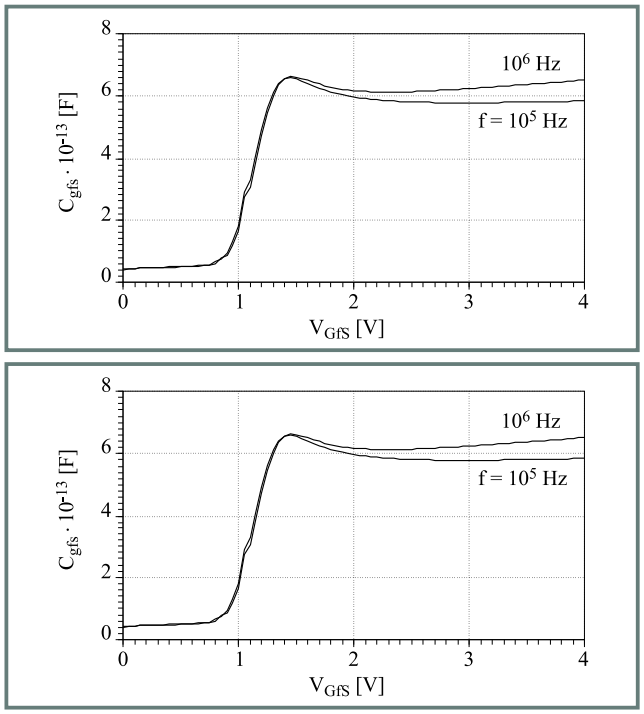


Fig. 7. $C_{gfs}(V_{GfS})$ determined experimentally. Device data: W = 100 µm, L = 10 µm, $t_{\mathrm{Si}} \approx 0.2$ µm, $t_{ox,b} \approx 0.4$ µm, $t_{ox,f} \approx 30$ nm, $N_B \approx 5 \cdot 10^{16}$ cm^{-3}.

experimentally observed effect of frequency variation. Such measurement in wider range of frequencies and for the set of devices should be done.

Preliminary numerical simulations of PD SOI MOSFET for varying frequencies (1 kHz, 100 kHz) were also done [8]. Figure 8 shows the obtained results. The parameters of the

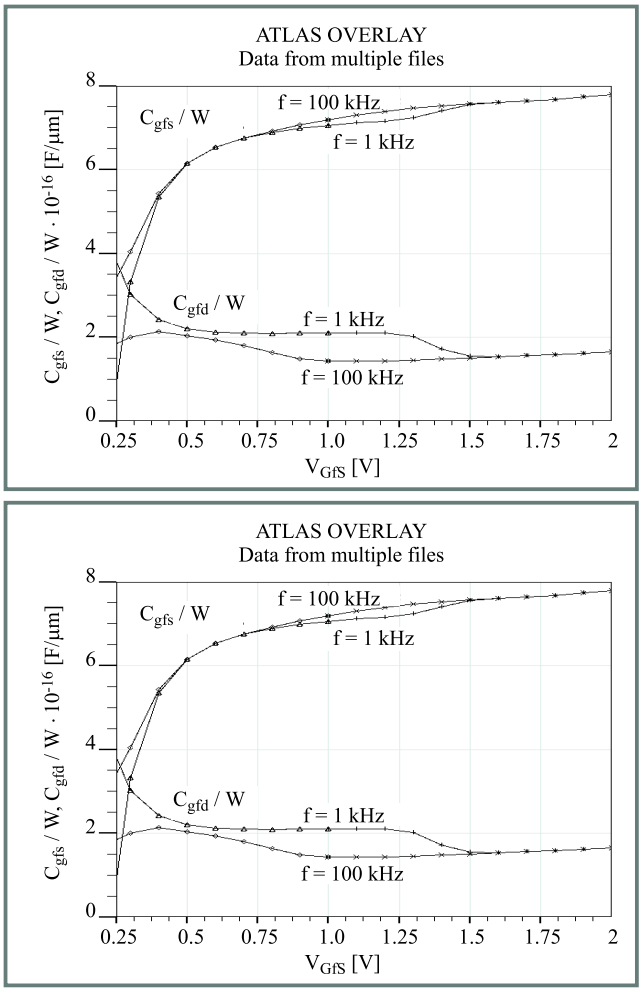


Fig. 8. $C_{gfs}(V_{GfS})$ determined numerically [8]. Device data: L = 0.6 µm, $t_{\mathrm{Si}} \approx 0.2$ µm, $t_{ox,b} \approx 0.4$ µm, $t_{ox,f} \approx 30$ nm, $N_B \approx 5 \cdot 10^{16}$ cm^{-3}.

simulated device are shown in the figure caption. The C_{gfs} and C_{gfd} data exhibit sensitivity to frequency variations in the saturation range, although the frequency range is much lower than above. However the data were obtained for the short-channel device. Thus phenomena in „pinch-off" region play much more important role, than in case of long-channel devices.

Both experimental and numerical data presented above confirm the need of accounting for frequency effect on C-V models of PD SOI MOSFETs.

7. Conclusions

The presented AC model of the PD SOI MOSFETs shows significant effect of frequency on device capacitances in strong inversion. Thus non-quasi-static approach to SOI MOSFETs small-signal modelling can be relevant for CAD of SOI CMOS analog and analog-digital circuits.

More general analysis of effect of frequency on MOSFETs admittances requires also accounting for transistors conductances.

The model should be extended towards higher frequencies range and improved in the subthreshold range.
In order to prove validity of the model extensive measurements and numerical simulations of PD SOI MOSFETs for wide range of frequencies should be done.

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