Paper

Comparison of microwave performances for sub-quarter micron fully- and partially-depleted SOI MOSFETs

Michaël Goffioul, Gilles Dambrine, Danielle Vanhoenacker, and Jean-Pierre Raskin

Abstract — The high frequency performances including microwave noise parameters for sub-quarter micron fully- (FD) and partially-depleted (PD) silicon-on-insulator (SOI) n-MOSFETs are described and compared. Direct extraction techniques based on the physical meaning of each small-signal and noise model element are used to extract the microwave characteristics of various FD and PD SOI n-MOSFETs with different channel lengths and widths. $TiSi_2$ silicidation process has been demonstrated very efficient to reduce the sheet and contact resistances of gate, source and drain transistor regions. 0.25 μm FD SOI n-MOSFETs with a total gate width of 100 μm present a state-of-the-art minimum noise figure of 0.8 dB and high associated gain of 13 dB at 6 GHz for V_{ds} = 0.75 V and $P_{dc} < 3$ mW. A maximum extrapolated oscillation frequency of about 70 GHz has been obtained at V_{ds} = 1 V and J_{ds} = 100 mA/mm. This new generation of MOSFETs presents very good analogical and digital high speed performances with a low power consumption which make them extremely attractive for high frequency portable applications such as the wireless communications.

Keywords — microelectronics, microwave devices, SOI MOSFET.

1. Introduction

The boom of mobile communications leads an increasing request of low cost and low power mixed mode integrated circuits. Maturity of silicon-based technology and recent progresses of MOSFET's microwave performances, explain the silicon success as compared to III–V technologies [1–4]. Silicon-on-insulator-based MOSFETs are very promising devices for multigigahertz applications. Especially low microwave noise at low drain voltage bias condition is one of very interesting high frequency characteristics of such devices. Moreover, due to the reduction of channel length dimension and the improvement of electrode processes (silicidation or metal T-gate processes), very low noise integrated circuits operating beyond 10 GHz and more are realizable. The main goal of this paper is to present state-of-the-art high frequency performances of sub-quarter micron gate length FD and PD SOI MOSFETs fabricated with a CMOS-compatible process on low-resistivity (20 Ωcm) SIMOX wafers.

Accurate knowledge of MOSFET noise parameters is required in performing realistic and reliable design of low noise amplifier (LNA), key element of high sensitive microwave receiver. In the present paper, we intend to accurately determine noise parameters of MOSFETs and to evaluate their dependence with the fabrication technology (fully versus partially depleted transistors).

In Section 2, bulk and SOI MOSFET's technologies are briefly described and compared. Details about the LETI SOI MOSFET's fabrication process are given in Section 3. Characterization techniques for the small-signal and high frequency noise model extractions are briefly described in Section 4. The measurement results of high frequency gains and noise parameters are presented in Sections 5 and 6, respectively.

2. MOSFET's technologies

The competing device technologies for the emerging mass-market applications are bipolar, CMOS, and mixed bipolar-MOS (BiCMOS). Bulk-silicon and silicon-on-insulator options are available for all three. Bipolar-only processes, and SiGe bipolar in particular, are high-performance technologies which are probably shooting too high with respect to the needs of the mobile communication market in the near future [5]. Bipolar-only processes target high-speed applications and are in particular not well suited for the implementation of the low-power digital base-band part of portable communication terminals. CMOS and BiCMOS are thus the best candidates for the single chip integration of mobile communication transceivers. High performance sub-micrometer-channel MOSFETs are capable of analogue operation at microwave frequencies [5]. The record transition frequencies of 150 GHz recently attained with experimental nanometer MOSFETs show that present-day MOS technology still has potential for improvement [6]. Using a SOI substrate, circuit speed can be substantially improved, but the ultimate advantage of SOI CMOS circuits is to be expected in low-power applications when using thin-film, FD SOI MOSFETs [7].

2.1. Bulk MOSFET

Characteristic of bulk technologies is that the transistors are fabricated directly on monocristalline silicon wafers and are thus all in contact with the substrate material. Bulk has been the main-stream technology for years, but SOI has now evolved into a mature contender [8]. A specific advantage of bulk technology is that the substrate acts as an efficient heat-sink, thanks to the high thermal conductiv-

ity of silicon. Bulk technology is however confronted with isolation problems. Bulk MOS transistors suffer from high parasitic capacitances – diffusion capacitances, body effect – and require special techniques for sub-micrometer scaling. Figure 1 shows the cross-section of a high-performance

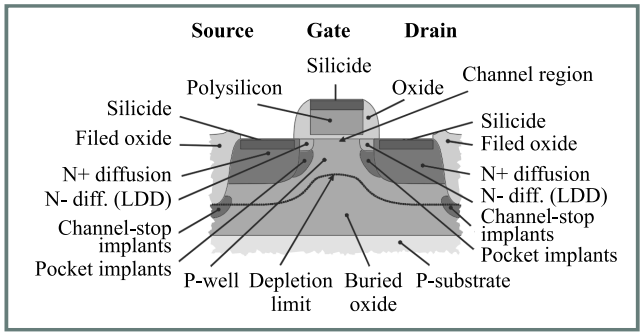

Fig. 1. Cross-section of a short-channel bulk-silicon MOSFET.

bulk MOSFET. The standard isolation technique in bulk technology is the use of reverse-biased junctions. This technique is only efficient at low frequencies and at moderate operating temperatures. Indeed, high-frequency signals may easily cross reverse-biased junctions because of the finite capacitance, while leakage currents increase rapidly with temperature up to a point where reverse biased junctions have little blocking effect. Junction isolation may even fail catastrophically when neighboring p- and n-wells combine to form a thyristor-like structure which can be triggered by a transient injecting a sufficient amount of current in any of the wells. These issues can be partly resolved by increasing the inter-well spacing, at the cost of a lower integration density, or by using advanced techniques such as trench isolation.

At low frequencies, when the substrate is essentially conductive, bulk MOSFETs are loaded by large capacitances due to the depletion region associated with the source and drain diffusions as well as with the inversion channel. The lower limit of the depletion region is represented in Fig. 1 by the dashed line. The presence of a large depletion region underneath the gate reduces the effective control of the gate on the channel. The off-state performance of bulk MOSFETs is also affected, as the gate voltage must be driven lower below threshold to restrain the leakage current below a specified level. Bulk MOSFETs must therefore be designed with higher threshold voltages.

The large depletion zones associated with the source and drain diffusions of bulk MOSFETs are also an obstacle to the sub-micrometer scaling of the channel length. Indeed, the finite width of these depletion zones set a lower bound on the channel length. Below this limit, the source and drain depletion zones overlap, creating a region where a strong electric field can sweep electrons directly from source to drain independently of the gate voltage. Even, at channel lengths above this punch-through limit, the source and drain depletion zones have a detrimental impact on scaling, as they contribute to lower the threshold voltage [7]. Present-day sub-micrometer MOSFET technologies compensate the punch-through and threshold voltage roll-off effects using special pocket implants, which are designed to locally divert the electric field [9]. These pockets must be very precisely located at the lower tip of the diffusions. To achieve the proper doping profile, a tilted implantation technique is used where the wafer is tilted at an angle with respect to the ion-beam. Four of these implants are required to provide pockets at the drain and source of MOSFETs aligned in two orthogonal directions. Specific masks are also required to select the implantation regions.

2.2. Partially depleted SOI MOSFET

Silicon-on-insulator technology can be used to enhance the performances of bulk MOSFETs, particularly speed and packing density. The latter is increased on SOI essentially thanks to the very efficient isolation of individual devices by the field and buried oxides. This all-round isolation alleviates the need for diffused wells which require specific contacts and careful spacing and are limiting the integration density in bulk technology. The buried oxide layer, with its low dielectric constant, contributes to significantly reduce the parasitic capacitances loading the source and drain diffusions, allowing SOI designs to book speed gains with respect to their bulk counter-parts [8, 10].

The partially depleted device shown in Fig. 2 is a rather conservative SOI MOSFET design: it is merely a bulk MOSFET transposed onto a SOI substrate. In particular,

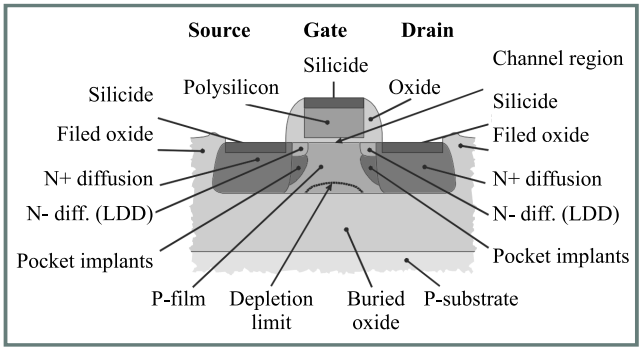

Fig. 2. Cross-section of a short-channel partially-depleted SOI MOSFET.

the existence of a quasi-neutral region below the depletion zone associated with the transistor ensures that the body effect in the partially depleted SOI MOSFET is identical to that of the bulk MOSFET, so that the SOI device shows no improvement in the subthreshold characteristics [7] which are essential for low-voltage applications.

2.3. Fully depleted SOI MOSFET

It has been shown in the last subsection that SOI technology remedies elegantly to the isolation problems of conventional bulk technologies and even contributes to circuit speed improvements. The use of fully depleted SOI MOSFETs extends the advantages of SOI even further to

easier down-scaling and nearly optimal low-voltage performances. Fully depleted SOI devices are obtained by using silicon film thicknesses thinner than the depth of the depletion zone, typically below 100 nm. Figure 3 represents the cross-section of a short-channel FD SOI MOSFET.

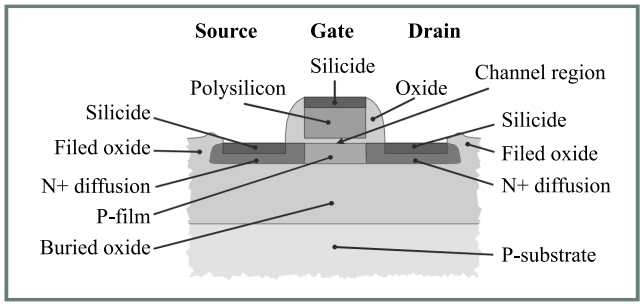

Fig. 3. Cross-section of a short-channel fully-depleted SOI MOSFET.

The very small body effect of fully depleted SOI MOSFETs is the key to their outstanding low-voltage performances and their good high-frequency performances. Interestingly, the fabrication of these devices is less complicated than that of bulk MOSFETs of comparable channel lengths, notwithstanding their better performances. The comparison of Figs. 1 and 3 shows indeed that the SOI MOSFET structure is inherently simpler than that of the bulk device.

In FD SOI MOSFETs, the small thickness of the silicon film strongly limits the extent of the depletion zones associated with source and drain, so that the risk of punch-through and the threshold-voltage roll-off are strongly attenuated. This feature alleviates the need for complex pocket implants, allowing to reach smaller channel lengths with a simpler fabrication process, comparatively to bulk technology. Even other short-channel effects such as channel-length modulation and drain-induced barrier lowering have been shown to be less severe in fully depleted SOI MOSFETs.

3. Fabrication process

200 nm UNIBOND wafers with a 400 nm buried oxide are used as the starting material. The silicon thickness is thinned down to 100 nm and 30 nm by a recessed-channel process, for partially- and fully-depleted SOI MOSFETs, respectively. Gate oxide of 4.5 nm is grown after a LOCOS isolation. A field implant is used to eliminate sidewall leakage. A 200 nm thick polysilicon layer is deposited and patterned by DUV lithography. A medium doped drain implant is followed by formation of a 80 nm spacer oxide after which the source-drain regions are implanted and activated with a 950°C/15 s RTA. A titanium silicide process is used to reduce the sheet and contact resistances of gates and the elevated 80 nm thick source-drain regions. After the silicide process a gate sheet resistance of about 10 $\Omega/\square$, instead of 100 $\Omega/\square$ for a classical doped polysilicon gate, is obtained for a 0.25 µm gate channel length MOSFET.

The back-end processing includes a three level metal process with tungsten plugs and planarization of intermetal oxides by chemical and mechanical polishing (CMP).

Figures 4 and 5 represent, respectively, the cross-section pictures of a PD and FD 0.25 µm SOI MOSFETs.

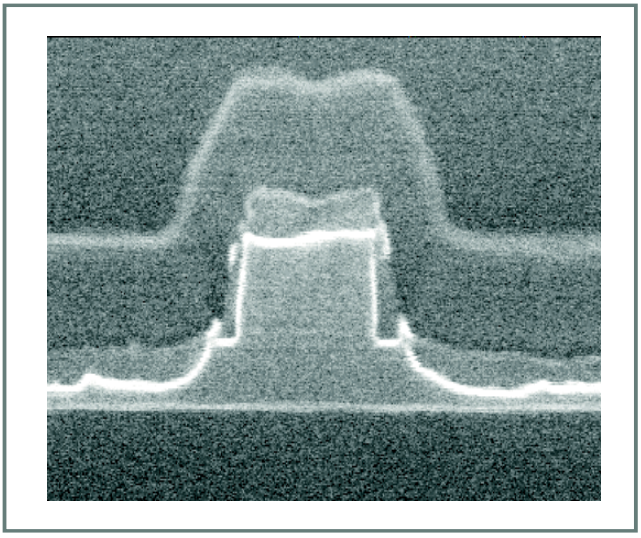

Fig. 4. Cross-section of a 0.25 µm PD SOI MOSFET (active silicon film of 100 nm) with a $TiSi_2$ silicidation process for the gate, drain and source areas.

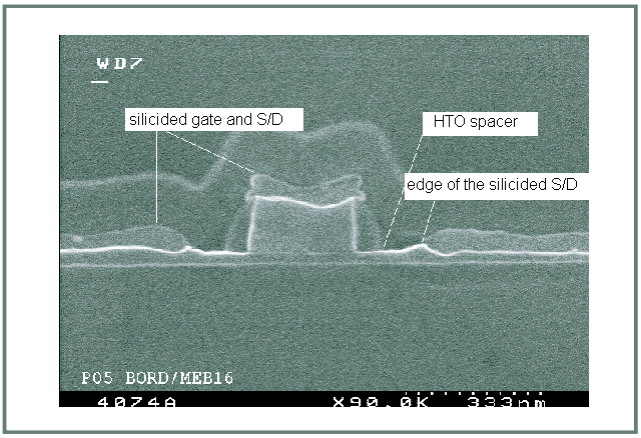

Fig. 5. Cross-section of a 0.25 µm FD SOI MOSFET (active silicon thin-film of 30 nm) with a recessed-channel process.

4. High frequency characterization techniques

The S-parameters were measured on-wafer up to 40 GHz (HP8510 network analyzer) and the noise figures in the $1 \div 18$ GHz frequency range (HP8971 noise measurement set-up).

The direct extraction methods presented in [11] have been applied to de-embed the transistors microwave performances from the on-wafer S-parameters measurements. This characterization procedure combines careful design of

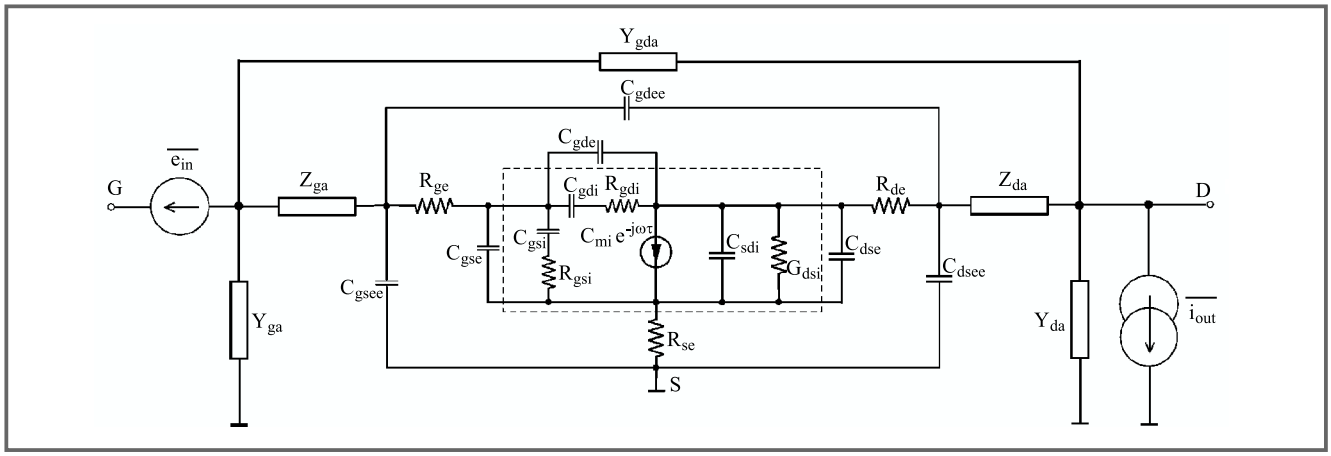

Fig. 6. Small-signal model including the input and output equivalent high frequency noise sources of a common-source SOI MOSFET.

probing and calibration structures, rigorous *in situ* calibration and a powerful direct extraction method. The extraction procedure is directly based on the physical meaning of each small-signal model element (Fig. 6). Knowing the qualitative small-signal behavior of each model parameter versus bias conditions, the high frequency equivalent circuit can be simplified for extraction purposes. Biasing MOSFETs under depletion, strong inversion and saturation conditions, the microwave small-signal elements and certain technological parameters can be extracted directly from the measured S-parameters. These new extraction techniques allow us to understand deeply the behavior of the sub-quarter micron SOI MOSFETs in microwave domain and to control their fabrication process. Moreover, due to the physical meaning attributed to each model element through the characterization process, the extracted equivalent circuit is scalable. This last point is crucial for circuits simulation and optimization purposes.

The four noise parameters are deduced from noise figures (NF_{50}), with a single 50 Ω generator impedance measured versus frequency [12] and the use of a two uncorrelated noise parameters model (e_{in} and i_{out}) represented in Fig. 6. Indeed, it can be shown that NF_{50} (in linear), in the case of FET, is a linear function versus frequency square in broadband. We can, then, obtain two independent noise parameters from the slope and the origin intercept of this linear function. By addind a two-uncorrelated noise sources model, all the FET's noise parameters (NF_{min}, R_n, $|\Gamma_{opt}|$ and $\arg(\Gamma_{opt})$) can be deduced. This noise model presented in Fig. 6 is a Pospieszalski based model applied to the extrinsic device. As shown Fig. 6, two noise uncorrelated noise sources are used: an input noise voltage source e_{in} and an output noise current source i_{out}. From these noise sources, two equivalent noise temperatures T_{in} and T_{out} are defined as follows:

$$T_{in} = \frac{\overline{e_{in}^2}}{4k\,\mathrm{Re}\left(\frac{1}{Y_{11}^E}\right)\Delta f}\,, \tag{1}$$

$$T_{out} = \frac{\overline{i_{out}^2}}{4k\,\mathrm{Re}\left(\frac{1}{Z_{22}^E}\right)\Delta f}\,, \tag{2}$$

$$\overline{e_{in}\,i_{out}^*} = 0\,, \tag{3}$$

where k is the Bolzmann constant, Δf is the bandwidth over which the noise is measured, $\mathrm{Re}\left(1/Y_{11}^E\right)$ is the input Thevenin equivalent resistance while $\mathrm{Re}\left(1/Z_{22}^E\right)$ is the output Norton equivalent conductance. It should be noted that experimental results [13] and models [14] show that the value of T_{in} is close to the ambient temperature and almost independent of the drain current while T_{out} is strongly dependent of the drain current and its value can be as high as 1000÷2000 K due to the hot electrons effect. These experimental and modeling studies have shown that the assumption of uncorrelated noise sources remains valid for drain current density less than 200/300 mA/mm. Using this noise measurement technique, the uncertainty of the extracted noise parameters depends both on the accuracy of the noise figure measurement with a 50 Ω generator impedance (about ±0.1 dB in the 2÷12 GHz frequency range) and on the validity domain of the noise model. This noise measurement technique has been compared [12] in many cases with commonly used the „multi-impedance" noise measurement method. This comparison has shown a good agreement between the four noise parameters obtained using our noise measurement method and commercially available system (based on the „multi-impedance" approach).

5. Small-signal high frequency performances

Table 1 shows the extracted values for extrinsic and intrinsic lumped small-signal elements for FD and PD SOI n-MOSFETs. These transistors have a gate channel length of 0.35 µm and are composed of 12 gate fingers of 6.6 µm connected in parallel, i.e. a total channel width of approximately 80 µm. A $TiSi_2$ silicidation process has been used

Table 1
Extracted values of extrinsic and intrinsic elements for FD and PD SOI n-MOSFET with a channel length of 0.35 µm and a total channel width of 80 µm at $V_{gs} = V_{ds}$ = 0.9 V

	C_{gsee}	C_{gdee}	C_{dsee}	C_{gse}	C_{gde}	C_{dse}	R_{se}	R_{de}	R_{ge}	C_{gsi}	C_{gdi}	G_{mi}	G_{dsi}	τ	R_{gsi}
	[fF]						[Ω]			[fF]		[mS]		[ps]	[Ω]
FD	5.77	5.77	10.4	14	16.5	6.5	4	13.7	5	90	12.5	22	1.1	0.75	7
PD	5.77	5.77	10.4	12.8	21.1	14	6.75	13.5	3.6	100	7	20	1.9	1	5

to reduce the gate, drain and source sheet resistivities and contact resistances.

The parasitic capacitive couplings between metallic interconnection located outside the active zone of the transistor (C_{gsee},C_{gdee} and C_{dsee}) are assumed identical for both types of SOI transistor (FD and PD). All of the extrinsic capacitances and resistances present extracted values fairly similar for both technologies, except for the extrinsic proximity drain-to-source capacitance C_{dse}. The augmentation of C_{dse} for the PD SOI MOSFET can be explain by the increase of the effective area of that parasitic capacitance due to the thicker active silicon film.

Better G_{mi} (10% more) and channel time delay τ (25% less) are observed for FD SOI MOSFET compared to the PD one. These improvements are explained by the better control of the channel region by the gate contact in the case of the FD structure. A reduction of the output conductance by approximately 42% is measured for the FD SOI MOSFET. The decrease of the output conductance indicates the reduction of the short channel effects with FD SOI MOSFETs.

The designers of RF circuits have defined some figures of merit for microwave transistors. If devices be used for RF applications, the aim has to be at maximizing the transit frequency (f_T) and maximum oscillation frequency (f_{max}), achieving a small minimum noise figure (NF_{min}) with a sufficiently high associated gain (G_{ass}), and reducing the $1/f$ noise.

Frequencies f_{max} and f_T are defined respectively as the cut-off frequency of unilateral gain (*ULG*) and the cut-off frequency of the current gain (H_{21}), i.e. f_{max} and f_T are the frequency points when, respectively, the *ULG* and H_{21} equal to 1 (i.e. 0 dB).

The maximum available gain (*MAG*) can be achieved for a stable device when we have simultaneously a complex-conjugate matched load and complex-conjugate matched source. The unilateral gain is defined by Mason [15] as the maximum available gain when a lossless feedback is used to cancel the transmission of power from the output to the input (S_{12}) of the device. *ULG* is derived from the S-parameters of the measured device as follows:

$$ULG = \frac{\frac{1}{2}\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)}, \tag{4}$$

where

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

with

$$\Delta = S_{12}S_{21} - S_{11}S_{22},$$

and k is the Rollett stability factor. The active device is unconditionally stable if $k > 1$ and potentially unstable if $k < 1$.

The current gain H_{21} is derived from the S-parameters of the measured device by

$$\left|H_{21}\right| = \frac{|i_2|}{|i_1|} = \left|\frac{-2S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}\right|. \tag{5}$$

¿From the small-signal equivalent circuit presented in Fig. 6, H_{21} and f_T can be expressed by the following simple equations:

$$\left|H_{21}\right| = \frac{G_{mi}}{\omega(C_{gs} + C_{gd})} \tag{6}$$

and then

$$f_T = \frac{G_{mi}}{2\pi(C_{gs} + C_{gd})}, \tag{7}$$

where G_{mi},$C_{gs}(= C_{gsi} + C_{gse})$ and $C_{gd}(= C_{gdi} + C_{gde})$ are, respectively, the intrinsic gate transconductance, the gate-to-source and gate-to-drain capacitances.

Sze defines a very useful relationship between f_{max} and f_T in [16]:

$$f_{max} = \frac{f_T}{2\sqrt{2\pi f_T R_{ge}(C_{gdi} + C_{gde}) + G_{dsi}(R_{ge} + R_{se} + R_{gsi})}}. \tag{8}$$

Approximate expressions (7) and (8) show that while f_T can simply be increased by scaling down the devices, f_{max} depends strongly on the parasitics, as well as on G_{mi} and G_{dsi} which are very sensitive to the drain current and thus V_{gs}.

Figure 7 presents the evolution of f_{max} and f_T as a function of the bias conditions ($V_{ds} = V_{gs}$) for silicided and non-silicided 12 x (6.6/0.35) µm^2 SOI n-MOSFETs. f_T and f_{max} of, respectively, 26 and 56 GHz are reached at $V_{ds} = = V_{gs} = 1$ V for the silicided 0.35 µm SOI n-MOSFET. These results render this type of devices suitable for low-voltage, low-power RF applications.

Cut-off frequencies f_T and f_{max} versus bias conditions curves reach a plateau above $V_{ds} = V_{gs} = 1.2$ V. This saturation characteristic can be explain by the saturation carrier velocity. In fact, for high values of longitudinal electric

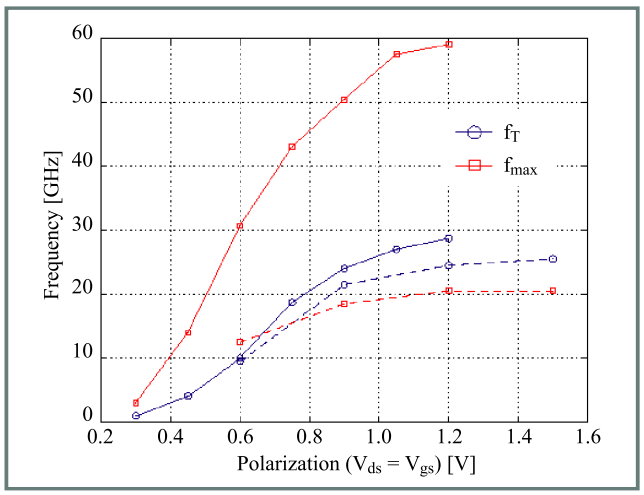

Fig. 7. Cut-off frequencies f_T and f_{max} as a function of supply voltage ($V_{ds} = V_{gs}$) for silicided (solid line) and non-silicided (dashed line) 12 x (6.6/0.35) µm^2 SOI n-MOSFETs.

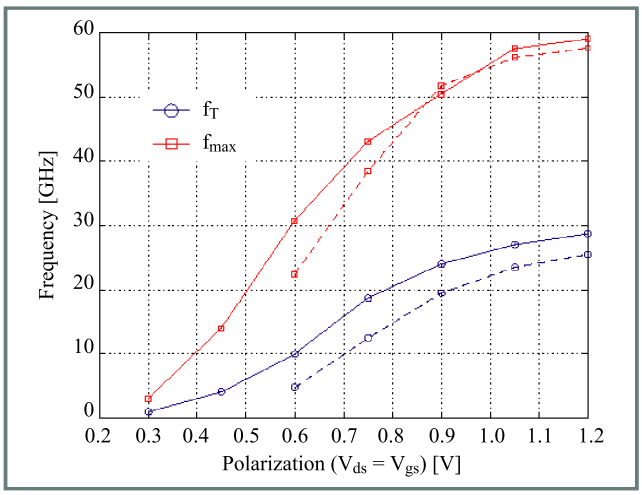

Fig. 8. Cut-off frequencies f_T and f_{max} as a function of supply voltage ($V_{ds} = V_{gs}$) for silicided FD (solid line) and PD (dashed line) 12 x (6.6/0.35) µm^2 SOI n-MOSFETs.

field between the source and drain electrodes, the velocity of the carriers in the thin inversion layer tends to saturate due to important collisions between them. These effects lead to an important degradation of the effective surface mobility of carriers in the channel. It is easy to understand that these effects are mainly observed in devices with small channel lengths. The saturation velocity of carriers in a MOSFET is reached for a longitudinal electric field between the source and drain, called critical electric field, of about 1 V/µm for electrons and about 3 V/µm for holes [17]. These values are in accordance with the measured characteristics presented in Fig. 7. We see that the velocity saturation effect is a very important limiting parameter in the design of small devices and thus particularly for microwave applications. Therefore, the study of the velocity saturation effect on the small-signal microwave performances of SOI MOSFETs is absolutely necessary to establish accurate and physical models.

Figure 7 shows clearly also the great interest of the silicidation process in order to improve the maximum oscillation frequency by reducing the parasitic extrinsic resistances R_{ge}, R_{de} and R_{se}. After silicidation, the parasitic extrinsic gate resistance is approximately reduce by a factor 10 and f_{max} is triple.

Figure 8 presents the evolution of f_T and f_{max} versus bias conditions for silicided FD and PD 12 x (6.6/0.35) µm^2 SOI n-MOSFETs. The slight improvement of cut-off frequencies obtained with FD SOI n-MOSFETs can be related to the improvement of the gate transconductance and the reduction of the ouput conductance and channel time delay previously mentionned in Table 1. The frequency band of the network analyzer being limited up to 40 GHz, the cut-off frequencies above that limit are determined by simple linear extrapolation of the corresponding gains in logarithmic graphs. Due to the measurements and extrapolations inaccuracies, an error of around 15% can be attributed to these extrapolated cut-off frequencies. That inacurracy can explain the similar values of f_{max} obtained for FD and PD SOI n-MOSFETs at higher bias conditions ($V_{ds} = V_{gs} > 0.7$ V).

Figure 9 presents the evolution of f_T and f_{max} versus the channel length of various silicided SOI n-MOSFETs having a total gate width (W) of 80 µm and biased at

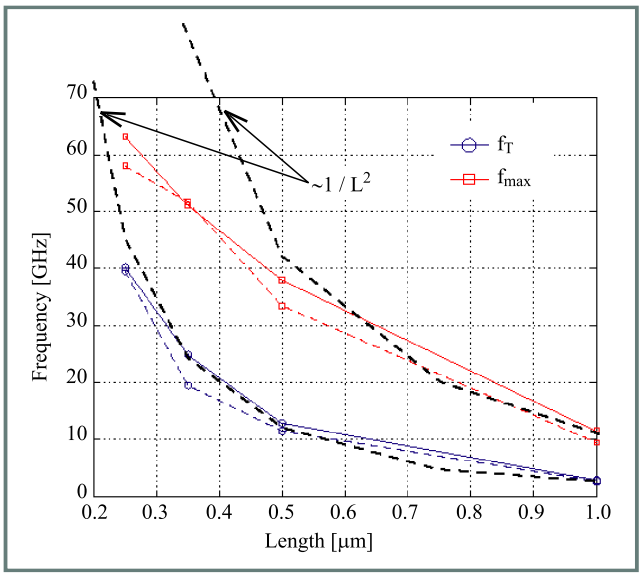

Fig. 9. Cut-off frequencies f_T and f_{max} versus channel gate length for 0.35 µm FD (solid line) and PD (dashed line) SOI n-MOSFETs at $V_{ds} = V_{gs} = 0.9$ V.

$V_{ds} = V_{gs} = 0.9$ V. The cut-off frequencies increase with the reduction of the channel length. The dependence in $1/L^2$ of f_T is in accordance with the simplified expression Eq. (7). In fact, G_{mi} being proportional to W/L and $(C_{gs}+C_{gd})$ to WL, f_T is a function of $1/L^2$. f_{max} presents also a dependence in $1/L^2$ for large channel lengths but this increase rate decreases for L smaller than 0.5 µm because of the R_{ge} increase with the reduction of the channel length (L) becomes dominant in Eq. (8).

6. High frequency noise characteristics

Accurate knowledge of transistor noise parameters ($NF_{min}, R_n, |\Gamma_{opt}|$ and $\arg(\Gamma_{opt})$) is required in performing realistic and reliable design of low noise amplifier (LNA), key element of high sensitive microwave receiver.

The main objective of this section is to compare the high frequency noise parameters for FD and PD SOI MOSFETs. More details about the physical interpretations of the measured high frequency noise parameters, but also the general interests and the limitations of SOI MOSFET technology for the realization of ultra-low-noise circuits can be found in [12].

Figure 10 represents the cut-off frequencies (f_T and f_{max}) and the minimum noise figure (NF_{min}) for a 0.25 µm FD SOI n-MOSFET with a current density of 100 mA/mm.

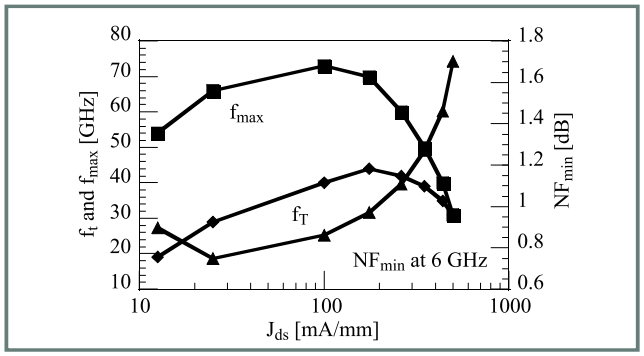

Fig. 10. Cut-off frequencies (f_T, f_{max}) and minimum noise figure NF_{min} versus current density at $V_{ds} = 1$ V for a 12 × (6.6/0.25) µm^2 FD SOI n-MOSFET.

A current gain cut-off frequency f_T and an extrapolated maximum oscillation frequency f_{max} of 40 GHz and 70 GHz, respectively, are reached at $V_{gs} = V_{ds} = 1$ V for a NF_{min} less than 1 dB.

Figure 11 shows the variation, at 6 GHz, of the NF_{min} and G_{ass} as a function of the drain current density ($V_{ds} = 1$ V).

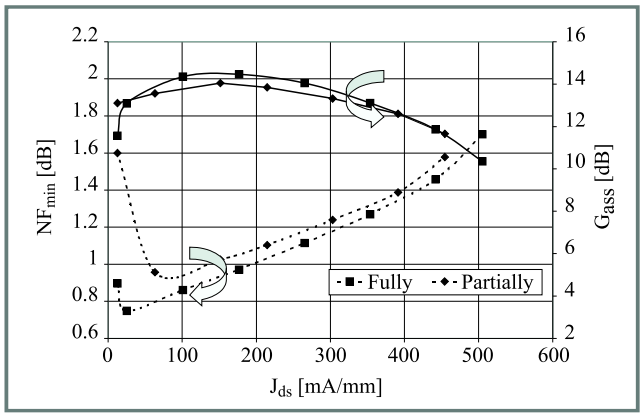

Fig. 11. Comparison between 12 x (6.6/0.25) µm^2 FD and PD SOI n-MOSFETs: evolution of NF_{min} and G_{ass} as a function of the drain current density at 6 GHz and $V_{ds} = 1$ V.

For a drain current density close to 75 mA/mm, the NF_{min} is 0.8 dB with G_{ass} of 13 dB. This result is one of the best reported in the literature. It shows that LNA could be designed with a power consumption of less than 35 mW/mm. Figure 12 presents the evolution, at 6 GHz, of the NF_{min} and G_{ass} as a function of the drain voltage for a constant drain current density of 75 mA/mm.

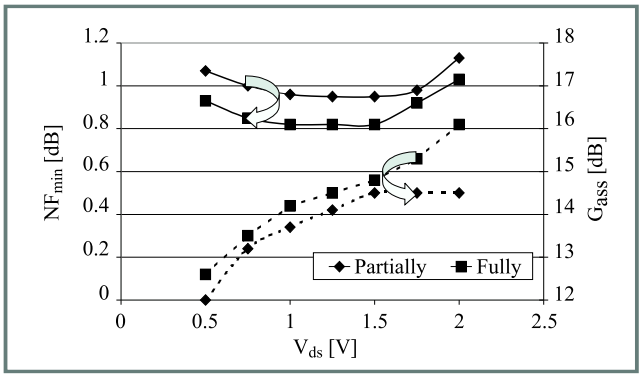

Fig. 12. Comparison between FD and PD SOI n-MOSFETs: evolution of NF_{min} and G_{ass} as a function of the drain bias voltage at 6 GHz; $J_{ds} = 75$ mA/mm; 12 x (6.6/0.25) µm^2.

Figure 13 shows the evolution of Γ_{opt} as a function of the drain current density at 2 GHz and $V_{ds} = 1$ V for 12 x (6.6/0.25) µm^2 FD and PD SOI n-MOSFETs.

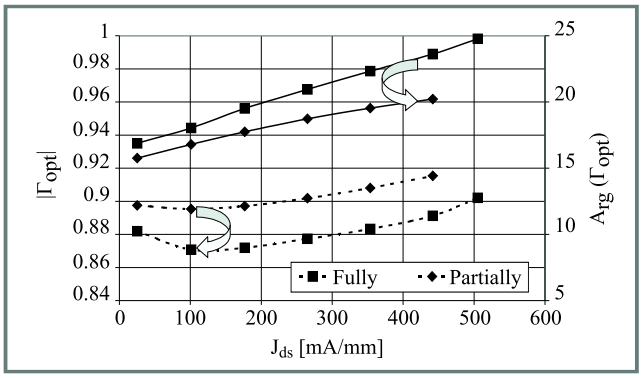

Fig. 13. Comparison between FD and PD SOI n-MOSFETs: evolution of Γ_{opt} as a function of the drain current density at 2 GHz; $V_{ds} = 1$ V; 12 x (6.6/0.25) µm^2.

By considering the very low value of NF_{min} at 6 GHz and its estimated measurement accuracy (±0.1 dB), the values and evolutions of NF_{min} for both FD and PD SOI transistors are similar. However, the extracted equivalent noise resistance R_n, which measures the sensitivity of the noise figure to change in the generator impedance, is slightly higher for PD SOI MOSFET (Fig. 14). More the value of R_n is low, more the minimum noise condition is easy to obtain in the case of LNA's design. As compared with a 0.6 µm channel length device [12], the value of R_n in Fig. 14 is three times lower.

Figure 15 represents the state-of-the-art results for different kinds of MOSFETs technologies. Low noise microwave performances of FD SOI MOSFETs appear to be ones of the best results reported in the literature.

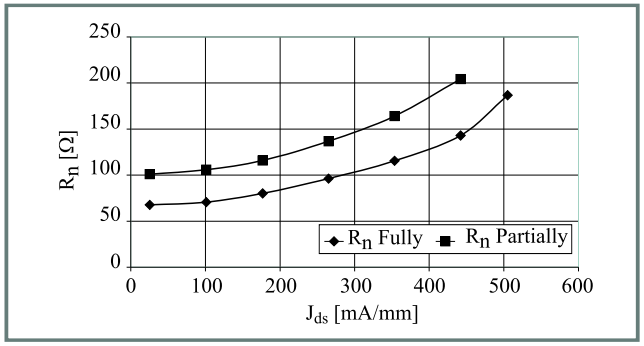

Fig. 14. Comparison between 12 x (6.6/0.25) µm^2 FD and PD SOI n-MOSFETs: evolution of R_n as a function of the drain current density at 6 GHz and V_{ds} = 1 V.

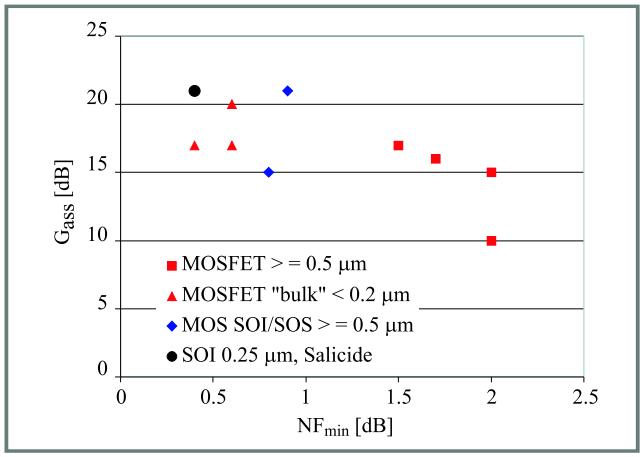

Fig. 15. State-of-the-art high frequency NF_{min} and G_{ass} for different published results of MOSFET technologies. Black dot corresponds to this work.

7. Conclusion

The microwave small-signal characteristics and the high frequency noise parameters for fully- and partially-depleted sub-quarter micron silicon-on-insulator MOSFETs are reported and compared. Slight improvements of nearly all small-signal and high frequency noise parameters are obtained with FD technology. Excellent microwave performances including high frequency noise have been obtained for 0.25 µm gate channel length FD SOI MOSFETs: a maximum extrapolated oscillation frequency (f_{max}) of 70 GHz and the state-of-the-art minimum noise figure (NF_{min}) of 0.8 dB with high available associated gain (G_{ass}) of 13 dB at 6 GHz, V_{ds} = 0.75 V, P_{dc} < 3 mW, have been measured.

These results render this type of devices suitable for low-voltage, low-power RF communication applications.

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