Paper

Design and Development of Miniature Dual Antenna GPS-GLONASS Receiver for Uninterrupted and Accurate Navigation

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Abstract—Global Positioning System (GPS), Global Navigation Satellite System (GLONASS), and GPS-GLONASS receivers are commonly used for navigation. However, there are some applications where a single antenna interface to a GPS or GPS-GLONASS receiver will not suffice. For example, an airborne platform such as an Unmanned Aerial Vehicles (UAV) will need multiple antennae during maneuvering. Also, some applications will need redundancy of antenna connectivity to prevent loss of positioning if a link to satellite fails. The scope of this work is to design a dual antenna GPS-GLONASS navigation receiver and implement it in a very small form-factor to serve multiple needs such as: provide redundancy when a link fails, and provide uninterrupted navigation even under maneuvering, also provide improved performance by combining data from both signal paths. Both hardware and software architectures are analyzed before implementation. A set of objectives are identified for the receiver which will serve as the benchmarks against which the receiver will be validated. Both analysis and objectives are highlighted in this paper. The results from the tests conducted on such a dual antenna GPS-GLONASS receiver have given positive results on several counts that promise a wider target audience for such a solution.

Keywords—dual-antenna receiver, embedded system, GLONASS, GPS, miniaturization.

1. Introduction

Typical single antenna navigation receiver architecture consists of a few critical blocks as shown in Fig. 1: RF front-end, correlator, and navigation processor [1], [2]. The RF front-end block consists of amplifiers, filters, down-conversion and Analog to Digital Converter (ADC) blocks for each of the signals. The ADC output is then relayed onto the correlator block, which generates the appropriate carrier frequencies and code bit streams in order to perfectly match with the incoming signal. The results of this process are passed on to the navigation processor, which estimates the location information. The navigation processor also generates appropriate messages to interface receiver with the host.

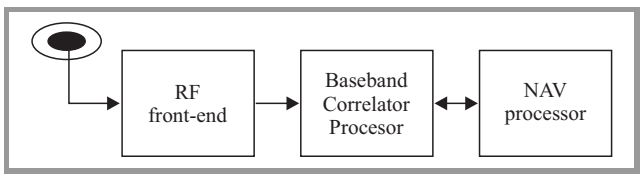


Fig. 1. Typical navigation receiver architecture.

Navigation receivers are available today in varied hues. There are both single constellation and multi-constellation receivers serving the needs of myriad user communities. GPS, GLONASS, and dual GPS-GLONASS receivers are commonly used for navigation. GPS is a USA satellite based navigation system providing reliable and uninterrupted location guidance services to global users [3], [4]. Launched in the 80's, it is one of the most popular navigation systems used world-wide across a multitude of applications. GPS is a typical single constellation receiver installed in mobile phones, PNDs, wireless base stations, and vehicles.

GLONASS is the Russian equivalent of GPS. Launched as a competitive system to GPS during the days of cold war, it went into degeneration during the disintegration of Soviet Union and was recently revived back to its full constellation. GLONASS has proven to be both an alternative as well as a companion to GPS for multi-constellation receivers. A multi-constellation receiver is slowly finding its relevance today with the stabilization of the GLONASS constellation. Typically, GPS is combined with GLONASS and offered as a higher performance platform, but at a premium value.

Most of today's navigation receivers are equipped with single antenna interface. However, there exists a niche segment that demands multiple antenna interfaces. An example would be that of an Unmanned Aerial Vehicle (UAV). UAVs today are used in several wartime applications. However, they have found their use in several civil and commercial applications as well. A few of them are: wildfire management, disaster management, pipeline and homeland security, and earth science research and applications.

The primary use of multiple antenna interfaces would be to have an uninterrupted navigation data even when the vehicle maneuvers. Navigation receiver's antenna need to have a clear view of the sky to catch the signals transmitted from the satellites. In vehicles such as UAVs, there is a high probability that a single antenna may not always see the sky and therefore continuous navigation may not be possible.

Another application that would greatly benefit the use of multiple antennas is that of in-vehicle navigation. In big cities with tall buildings, a single antenna may have a limited sky view. With a two antenna architecture with an antenna each placed on the dash and on the rear parcel tray enables more coverage of the sky and leads to a higher percentage of navigation guidance.

During a study of past and current developments, it has been found that most receivers are developed to address a single parameter such as multipath, interference mitigation or redundancy. These receivers are high-end and targeted at very specific applications.

The challenge now is to come up with a new architecture that can support multiple antennas, build system redundancy, and provide improved navigation availability, lower power consumption and a miniature form-factor package. The receiver incorporates two independent channels to receive dual-frequency signals simultaneously.

There are receivers with multiple antenna interfaces and multi-constellation architectures [6]–[8], but these are designed to address a different class of applications. For instance, the solution proposed to overcome severe vehicle maneuvering in GPS receivers is discussed in [6] where a GPS receiver is connected to 3 GPS antennas through a RF switch. The RF switch is controlled using software to periodically sample the signal from each path in order to determine the signal availability and quality. This approach avoids duplication of the signal processing blocks, but can take more time for a position fix. Again, the multiple antenna solutions in [6] and [7] are more driven towards multipath mitigation using antenna array technology.

The work given in [8] presents combined GPS and GLONASS receiver for consumer market. A fully integrated dual-channel reconfigurable GNSS receiver supporting Compass/GPS/GLONASS/Galileo systems is implemented in 65 nm CMOS semiconductor technology [9]. The target multi-system GNSS receiver architecture based on an PCI ExpressCard peripheral card for the PC computer is described in [10]. The work given in [11] presents a practical design of smart antenna system for GPS/GLONASS anti-jamming based on adaptive beamforming.

The authors have noticed very few works on such designs in a small foot-print. Hence, GPS-GLONASS navigation receiver is designed and developed in a very small form-factor to serve the multiple needs such as:

– provide redundancy when one link fails,

– provide uninterrupted navigation even under maneuvering,

– provide improved performance by combining data from both signal paths.

The rest of the paper is organized as follows. The multi-constellation GNSS (GPS-GLONASS) versus stand-alone GPS or GLONASS is debated in Section 2 along with a glimpse into the architecture proposed and implemented for a miniature multi-antenna navigation receiver. Hardware and software implementation details of the receiver are presented in Section 3. Measurements and results are given in Section 4, and the conclusion is presented in Section 5.

2. Proposed Dual Antenna GNSS Receiver Architecture

Multiple-constellation GNSS receivers offer significant performance advantages over single constellation receivers in almost all positioning applications. Increased availability, improved accuracy, and less susceptibility to jamming are ones that are readily apparent. With the exponential increase in the number of GPS receivers deployed in conditions where the satellite visibility is limited, a multiple-constellation receiver can continue to provide fairly accurate positioning even when a GPS-only receiver is unable to do so, resulting in a much more satisfactory user experience.

Until recently, GPS was the only satellite based navigation system with full operational capability. However, the GLONASS constellation has also reached its full deployment configuration. The main advantage of having multiple satellite constellations is in the availability of more satellites and improvement in Geometric Dilution of Precision (GDOP) [5]. The GNSS receiver by virtue of tracking more number of satellites is capable of providing a faster time to fix. In addition, a stand-alone (single constellation) receiver may not be able to compute a position fix in situations where the antenna is obscured, but with a multi-constellation GNSS receiver, it is highly probable that the combination of the available satellites from different satellite constellations can provide a navigation solution.

The multi-constellation GNSS receiver architecture proposed involves two independent RF and base-band processing paths. Each of the two independent paths can act as a stand-alone GPS-GLONASS position engine. This dual RF processing maximizes the satellite availability during vehicle maneuvers or signal blockage. This in turn, ensures near complete visibility of all the satellites from both the constellations and hence increases the probability of a faster time to fix.

The GNSS receiver architecture is depicted in Fig 2. As seen, there are two antenna paths with each path supporting a GPS and a GLONASS RF front-end (GLSRF and GPSRF). The output of the GPS front-end is fed to the GPS correlator and that of the GLONASS front-end to the GLONASS correlator. It is obvious that there are two such correlator pairs, one for each signal path. The data from all four paths are fed to the navigation processor where the

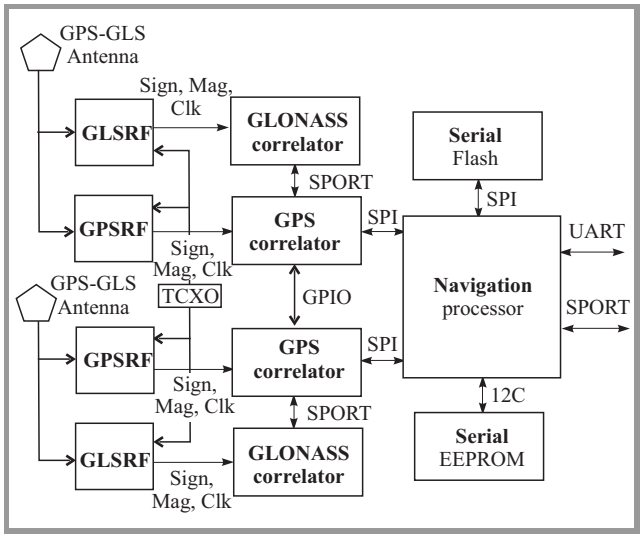


Fig. 2. Dual-antenna GPS-GLONASS receiver architecture.

data is decoded and the navigation data is computed. In addition to the main components described above, there are other important blocks that contribute to making a complete receiver. The memory is interfaced to the navigation processor and serves two important purposes – holds the boot program for the baseband correlators and navigation processor and stores the runtime configuration and satellite data.

In the proposed receiver architecture, the design is optimized to balance the trade-off between the factors as: components size, performance, consumed power and cost.

3. Hardware and Software Details of GNSS

3.1. Hardware Implementation

With reference to the receiver block diagram in Fig. 2, hardware details are provided. Each antenna port is immediately followed by a power splitter. The power splitter matches the impedance to 50 Ω at both its input and output. The two output ports from each splitter feed the front-ends of a pair of GPS and GLONASS RF chips. The down conversion of L1 frequency is performed in a single mixer stage to generate IF frequencies in each RF chip. The local oscillator frequency required for mixing operation is derived from a common reference clock. The final output from the RF front end is a digitized IF signal.

The digitized IF signal is separately processed in GPS and GLONASS base-band processor blocks. This feature is duplicated across two paths resulting in dual independent base-band processing of the signal received from the two antennas. The respective baseband processors work on the IF outputs from the RF chips, run signal acquisition and tracking algorithms, receive the data bits from the satellites and deliver the results to the navigation processor.

The key hardware specifications of the RF front end are listed in the Table 1 (QFN denotes "quad-flat no-leads" plastic package, and RLC denotes resistors and inductors and capacitors). The digitized IF signal is separately processed in GPS and GLONASS base-band processor blocks. This feature is duplicated across two paths resulting in dual independent base-band processing of the signal received from the two antennas. The respective baseband processors work on the IF outputs from the RF chips, run signal acquisition and tracking algorithms, receive the data bits from the satellites and deliver the results to the navigation processor. The key hardware specifications of the baseband processors are shown in Table 2 (FBGA means "Fine pitch Ball Grid Array"). The navigation processor in turn intelligently weighs the measurements and computes the navigation solution in three modes: GPS only position, GLONASS only position, and GPS-GLONASS combined position. The key hardware specifications of the navigation processor are listed in Table 3. The navigation processor has adequate internal memory and hence the only memory device required to hold the boot program is a Flash memory. A serial Flash is selected in order to minimize the package area and avoid PCB routing of address and data bus. The key hardware specifications of the memory are presented in Table 4. The receiver provides several industry standard interfaces such as Universal Asynchronous Receiver Transmitter (UART), Serial Peripheral Interface (SPI), Serial Port (SPORT) and two-wire synchronous interface thereby providing multiple options for connectivity with the host system. The key specifications of the interface section are shown in Table 5. The power supply

Table 1
Key specifications of the RF front-end

Size	4 × 4 mm
Package	QFN, 24-lead
Number of external components	23 RLC
Occupied PCB area	9 × 9 × 4 mm

Table 2
Key specifications of baseband processor

Size	7 × 7 mm
Package	FBGA, 24-lead
Number of external components	11 RC
Occupied PCB area	8 × 8 × 2 mm

Table 3
Key specifications of navigation processor

Size	7 × 7 mm
Package	FBGA, 24-lead
Number of external components	11 RC
Occupied PCB area	7 × 7 × 1 mm

Table 4
Key specifications of memory

Size	6 × 4 mm
Package	DSM, 24-lead
Number of external components	4 RC
Occupied PCB area	7 × 5 × 1 mm

Table 5
Key specifications of interface

UART	115200 b/s, 8 data bits, 1 start bit, 1 stop bit
SPI	22.5 Mb/s, 16-bit data interface, full-duplex
Synchronous interface	40 MHz half duplex
Serial port (SPORT)	22.5 MHz full duplex

to the hardware should be able to supply 1.5 A at 3.3 V. On-board, the power supply section converts the input voltage of 3.3 V into 1.2 V and 2.5 V to supply the core of the different chips. The key hardware specifications of the power supply section are listed in the Table 6 (DFN indicates "Dual flat no leads" package). The PCB is a crucial hardware component that determines the receiver size. The PCB should be small enough to meet the constraint of miniaturization, but should not impose severe penalties in terms of using expensive PCB manufacturing technologies. The PCB should support mechanical structures such as RF connector, interface connector and an enclosure.

Table 6
Key specifications of power supply

Size	4 × 3 mm
Package	DFN, 12-lead
Number of external components	12 RLC
Occupied PCB area	7 × 9 × 2 mm

3.2. Software Implementation

The presence of multiple processing elements in the design brings with it the challenges for the software in terms of performing the power on initializations for each processor, managing the inter-processor communication, weeding out the unwanted measurement from the several that enter the receiver and finally managing the man-machine interface through one of the many interfaces on the receiver. Figures 3 to 6 depict flowcharts for initialization, inter-processor communication, boot sequence program, and measurement.

Upon power up, each of the four processing elements comprising of the two baseband processors, the navigation processor and the FPGA will need to be initialized with their respective programs. Since the entire system has a single Flash memory, the individual program files are allocated specific segments. The Flash is interfaced with the navigation processor and upon power up, the boot program is brought into the navigation processor.

The boot program sequentially manages the initialization by bring in the program of each processing element in turn and then transferring the same to the corresponding processor. In addition, once a processor is loaded with its program, it should not immediately start executing. It is important to maintain synchronization with the other processors and towards this, signaling is performed to ensure that all processors start at the same instant. Once the system is up

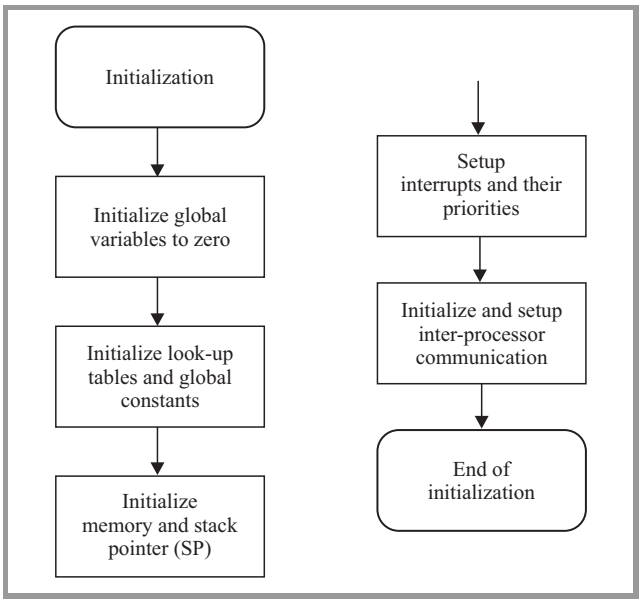


Fig. 3. Initialization.

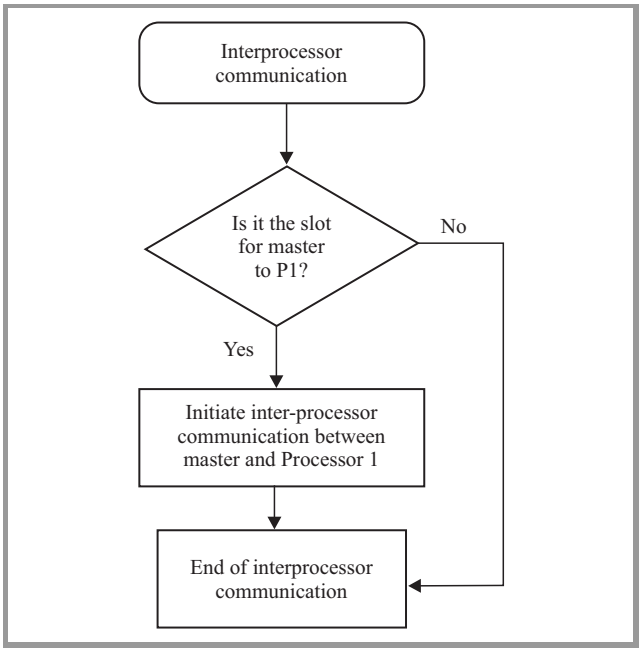


Fig. 4. Interprocess communication.

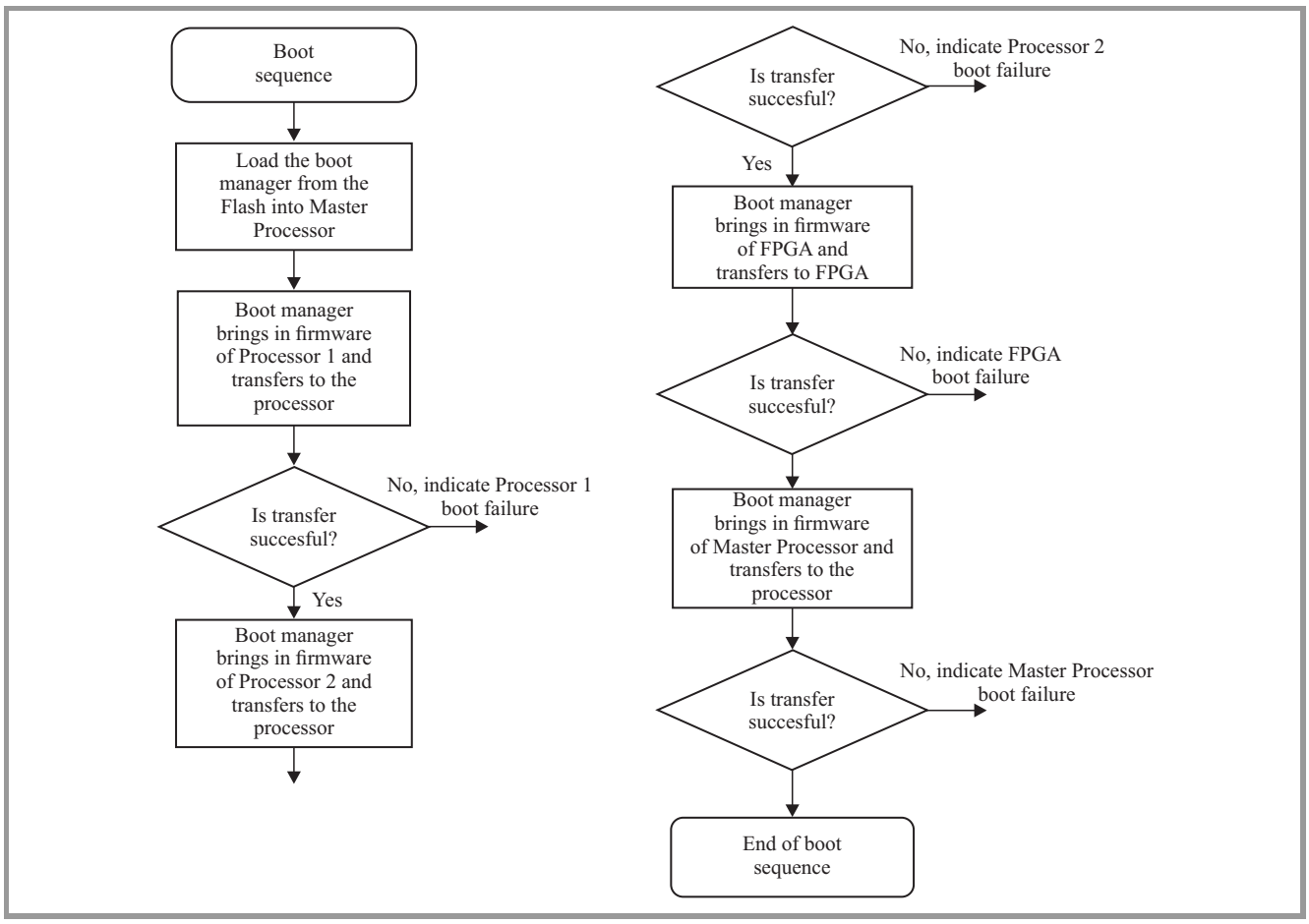


Fig. 5. Boot sequence.

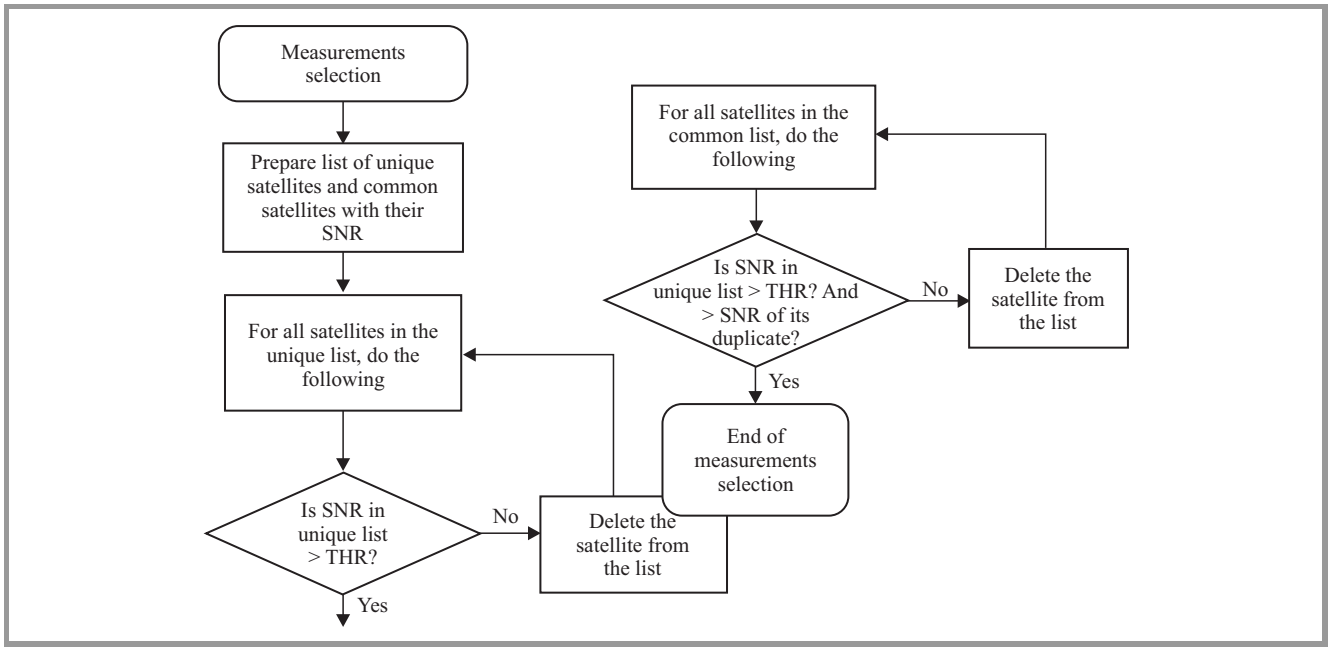


Fig. 6. Measurement selection.

and running, it is important to seamless exchange data between the different processing entities. The results from the signal processing have to be passed from the correlators to the navigation processor while any configuration to be done from the navigation processor is passed back to the correlators. This happens through the SPORT interface, which is programmed to work as SPI. In a dual-antenna system, the number of measurements is double that of a single antenna system. Further, some of the satellite signals enter through both antennas and arrive with different characteristics. It is important for the navigation processor to apply selection criteria to reject the unwanted measurements. The simplest and reliable means of discarding a measurement is to look at the signal level of the measurement. A threshold can be set based on experiments and any measurement whose signal level falls below the threshold can be rejected. Finally, the navigation solution computed in the receiver has to be brought out and delivered to the other entities which are part of the bigger system. The receiver has multiple interfaces to address such needs – UART, SPI, and synchronous communication. The UART is normally used to connect to a PC. The SPI and synchronous communication interfaces are more suited for embedded interfaces where the inter-connection happens between two or more processors.

4. Measurements and Results

To validate the dual antenna GPS-GLONASS receiver, several tests were conducted to justify the creation of such a receiver. Some of the key measurements and results are presented in this section.

4.1. Size

The miniature dual antenna GPS-GLONASS receiver is realized using indigenous as well commercial-off-the-shelf components. The design is implemented in a tiny $40 \times 40 \times 1$ mm (length $\times$ width $\times$ height) form-factor with dual row 50-pin connector for data and power supply interfaces along with the two antenna ports. A snapshot of the receiver module is shown in Fig. 7.

Fig. 7. Miniature dual antenna GPS-GLONASS receiver.

4.2. Power Consumption

The power consumption was measured by connecting a GPS-GLONASS antenna to each of the two ports and allowing the receiver to capture as many satellites as possible and computing the navigation solution. The current consumed was measured at multiple instances over a 12 hour period and the average of the current consumed was recorded. The current was measured to be 310 mA which amounts to a shade over 1 W. This result is encouraging as it enables the receiver to be used across several applications where power consumption is important.

4.3. Time to First Fix

The Time to First Fix (TTFF) is an important factor of a receiver. This indicates the speed at which the receiver is able to lock onto satellites and deliver the navigation output. The test setup consisted of the following: dual antenna GPS-GLONASS receiver, GPS-GLONASS antennae, and host PC to process the receiver output. The test results were recorded under open sky conditions. It can be seen in Table 7 that the TTFF in the combined mode is better than the worst case seen in a stand-alone receiver.

Table 7
Time to first fix for receivers

TTFF	Trial [s]	Trial 2 [s]	Trial 3 [s]
GPS	32	34	27
GLONASS	23	18	35
GPS-GLONASS	30	31	34

4.4. Accuracy

Using the same test setup, another important parameter was measured – position accuracy as shown in Fig. 8. The navigation data output from the receiver was recorded for over 24 hours with the antenna kept under a clear sky view. The plot of the position coordinates from GPS-only, GLONASS-only and combined modes are plotted in the same graph.

4.5. Field Test

Another test conducted on the receiver was a field test. Here, the advantage of having two antennas was exploited. The test setup consisted of the following: dual antenna GPS-GLONASS receiver, Stand-alone GPS receiver, GPS-GLONASS antennae with splitter, and host PC to process the receiver output. The objective of this test is to justify the presence of multiple constellation and dual antenna interface on the receiver. The receiver is installed in a vehicle with the two antennas placed on the dash and rear parcel tray respectively. A stand-alone high performance GPS receiver is also used in the test and the antenna placed on the dash is connected to this receiver through a splitter. The

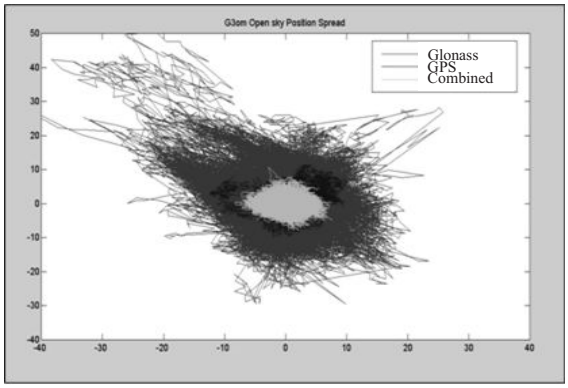
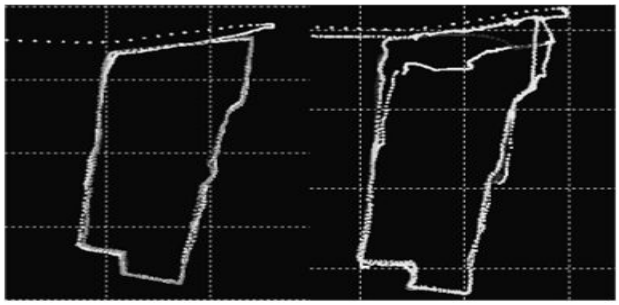


Fig. 8. Position accuracy.

vehicle is driven in a designated test route with buildings on either side of a narrow street. The performance of the receivers is compared and the plot from the test is shown in Fig. 9. The test results in Fig. 9, clearly demonstrates



Position plot from dual antenna GPS-GLONASS receiver | Position plot from a stand-alone GPS receiver

Fig. 9. Position trace from field test.

the benefits of satellites increased availability in the dual-antenna GPS-GLONASS combined mode. As a result, the plot of the receiver on the left looks much clean compared to the plot shown on the right for a GPS-only receiver. The field tests were conducted in a land-vehicle by placing one antenna on the dashboard and another on the rear parcel tray. When the vehicle moves in a narrow lane with reasonably tall buildings on either side, the satellite visibility is mostly restricted in the direction of vehicle. With a single antenna single constellation receiver, the number of satellites that are visible is limited to a single constricted view (either out of the front pane or the rear pane. A dual antenna multi-constellation receiver has the advantage of increased number of satellites from two constellations and also of seeing two different views out of the front and rear of the vehicle.

5. Conclusions

The key takeaway from this work is the realization that a multiple constellation receiver is better than a single constellation receiver. Further, dual-antenna multiple constellation receiver performs better than a single-antenna multiple constellation receiver.

The dual-antenna GPS-GLONASS receiver has no peers as it is a unique design in its class of receivers. It is designed to be a miniaturized receiver that is capable of being integrated into several classes of applications.

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