Invited paper

SOI nanodevices and materials for CMOS ULSI

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Abstract— A review of recently explored new effects in SOI nanodevices and materials is given. Recent advances in the understanding of the sensitivity of electron and hole transport to the tensile or compressive uniaxial and biaxial strains in thin film SOI are presented. The performance and physical mechanisms are also addressed in multi-gate Si, SiGe and Ge MOSFETs. The impact of gate misalignment or underlap, as well as the use of the back gate for charge storage in double-gate nanodevices and of capacitorless DRAM are also outlined.

Keywords— ballistic transport, gate misalignment, GIFBE, mobility enhancement, SOI, strain engineering, tunneling current.

1. Introduction

The silicon-on-insulator (SOI) devices are the best candidates for the ultimate integration of ICs on silicon. The flexibility of the SOI structure and the possibility to realize new device architectures allow optimum electrical properties to be obtained for low power and high performance circuits. These transistors are also very interesting for high frequency and memory applications [1–3]. In this paper, an overview of recently explored new effects in advanced SOI devices and material is given. The advantages and drawbacks of a number of new device architectures are also addressed.

2. Physical mechanisms in advanced SOI MOSFETs

Ultra-thin gate oxide (sub-2 nm) leads to direct gate tunneling currents [4] that consist of three main streams of carriers (Fig. 1). In partially-depleted (PD) SOI MOSFETs, the floating body of the device is isolated by the buried oxide (BOX) and charged by the direct tunneling currents, J_{EVB} and J_{HVB}. When a floating-body device is biased in inversion, the body is mainly charged by a hole current resulting from the tunneling of valence band electrons into the gate ($J_{HVB} \ll J_{EVB}$). When biased in accumulation, the body is charged with electrons coming from the gate conduction band. These currents strongly affect the body potential of the PD devices, giving rise to gate-induced floating body effect (GIFBE). The different gate current contributions are plotted in Fig. 1 to illustrate the body-charging mechanism.

A direct consequence of the GIFBE is the sudden increase of the drain current characteristics for V_G close to 1.1 V.

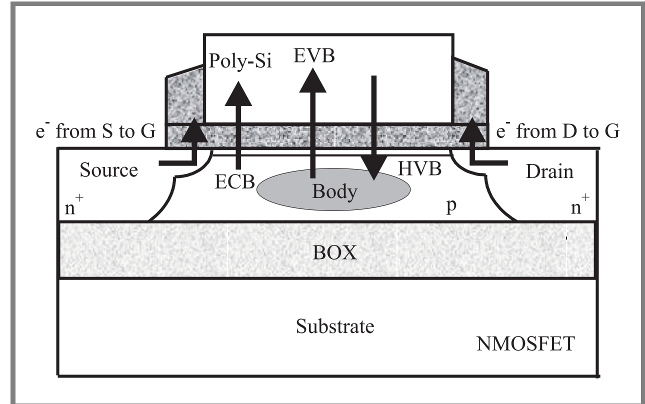

Fig. 1. Tunneling current components in a NMOSFET. Explanations: EVB – valence band electron tunneling, ECB – conduction band electron tunneling, HVB – valence band hole tunneling.

For this voltage, the gate-to-body current (I_{GB}) charges up the body and the drain current increases. This "kink-like" effect gives rise to a strong second peak in transconductance (up to 40% increase), which clearly appears in Fig. 2 for low drain bias. This figure illustrates the influence of the gate size on the GIFBE's amplitude and position. The voltage corresponding to the onset of the 2nd peak of transconductance (G_m) is nearly independent of the gate length (and width) whereas the amplitude of the peak depends on the device geometry. The 2nd peak is clearly reduced as the gate length (or width) are shrunk down. It is usually reported that floating body effects (FBEs) are reduced in short-channel devices by enhanced junction leakage or in narrow-channel devices by

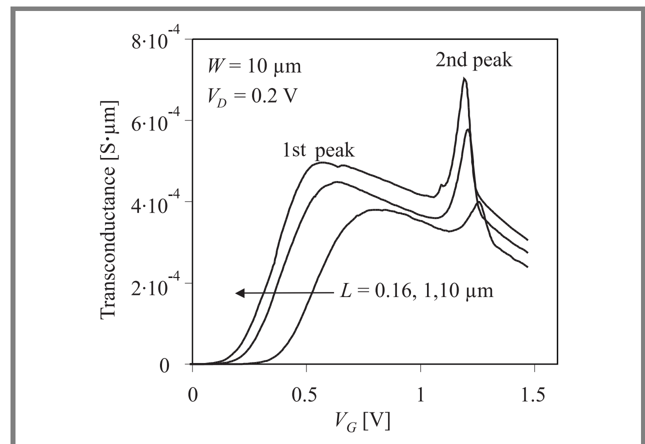

Fig. 2. Normalized transconductance of a 10 μm wide NMOSFET versus gate bias for various gate lengths.

increased recombination rate near the sidewalls. In both cases, the removal of majority carriers from the body is more efficient, hence the body charging by I_{GB} is less effective and the GIFBE is reduced. However, even in the smallest transistor, where both junction and sidewall contributions occur, the role of the gate tunneling current remains significant.

The drain power spectral density also presents a special behavior [4]. For V_G values inferior to the GIFBE onset gate voltage (around 1.1–1.2 V), conventional $1/f$ noise is observed, attributed to carrier fluctuations from the inversion layer due to carrier trapping/detrapping in the vicinity of the silicon/SiO_2 interface. Nevertheless, an excess noise occurs, characterized by the superposition of a Lorentzian-like component on the $1/f$ noise when the GIFBE is present. Similarly to FB PD SOI devices in saturation mode, a flat plateau is followed by a $1/f^2$ roll-off at a given corner frequency. In this case, the corner frequency shifts to higher frequencies as the drain bias increases: here, the front gate bias plays the role of the drain bias, and we have a similar behavior with frequency as the Kink-related excess noise.

From more than two decades for $L = 10$ μm, the excess noise decreases down to only one decade or less, and becomes almost insignificant for short devices ($L = 0.20$, 0.12 μm). Figure 3 represents the calculated ratio between the maximum drain current power spectral density ($S_{Id\,\max}$) and the minimum one ($S_{Id\,\min}$, value of the plateau at low V_G without GIFBE).

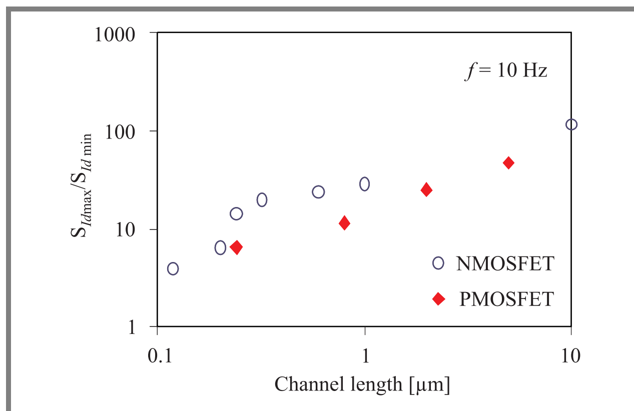

Fig. 3. Ratio between the maximum drain current noise ($S_{Id\,\max}$) and the minimum one ($S_{Id\,\min}$, value of the plateau at $V_G = 0.9$ V) for N- and PMOSFETs.

Two general features may explain the obtained results. On the one hand, the magnitude of the second transconductance peak is reduced as the channel length is shortened (FBEs are usually lowered by enhanced contributions from junctions), and the role of the gate current is partially offset, so that we notice a reduced contribution of the G_m 2nd peak on the noise overshoot. On the other hand, reducing the channel length causes an enhancement of the $1/f$ noise level, and this higher noise level probably masks the excess noise due to the GIFBE.

The GIFBE in a twin-gate (TG) structure (Fig. 4) is significantly reduced [5].

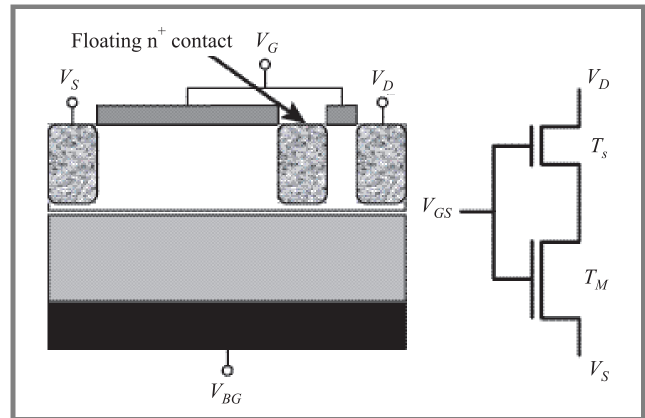

Fig. 4. Twin-gate NMOSFET.

In particular, the impact of the TG structure is pronounced on the Lorentzian noise overshoot (Fig. 5). Such a reduction results from a lowering of the part of the EVB current that reaches the source junction (the holes from the slave part (T_s) of the TG device are screened from reaching the source by recombination at the inner n^+ contact).

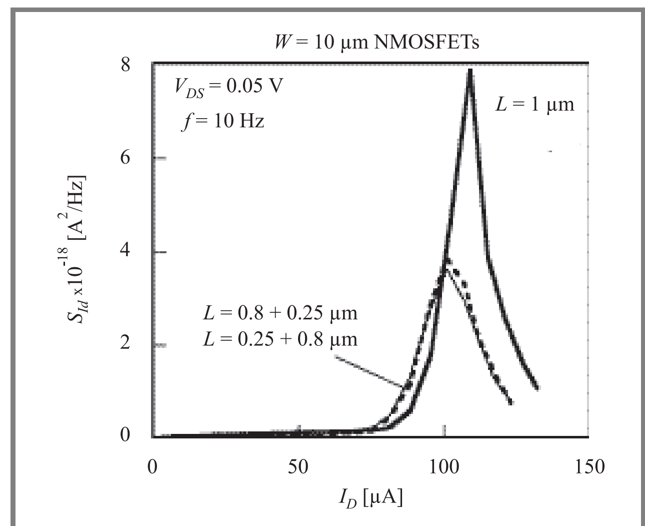

Fig. 5. Spectral density of drain current noise (S_{Id}) versus drain current (I_D) for NMOSFET (bold line) compared with the two TG combinations.

A GIFBE is also observed in fully depleted FinFET when a back gate bias is applied leading to an accumulation at the bottom of the fin (Fig. 6) [6].

In a double gate MOSFET, the application of a back gate voltage can lead to a volume inversion and to a screening reducing the number of trapped carriers in the gate oxides. This phenomenom induces a reduction of the low frequency noise (Fig. 7) [7].

The self-heating effect is also a harmful parasitic effect in SOI. The traditional buried silicon dioxide has a poor thermal conductivity that leads to an enhancement of the chan-

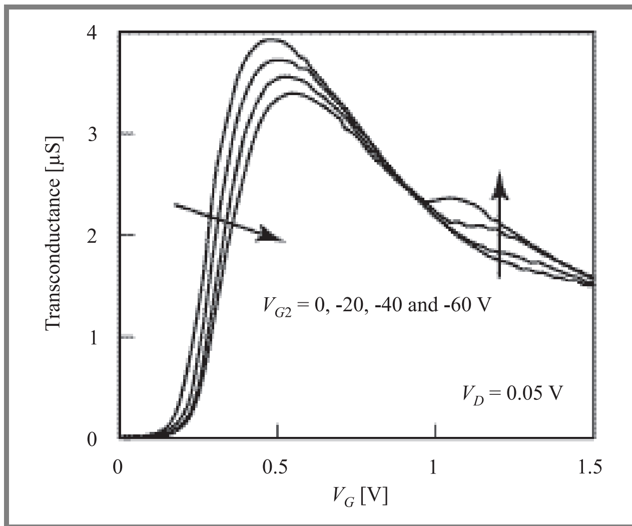

Fig. 6. Measured transconductance of a FD FinFET for different values of back gate bias ($L = 10$ μm).

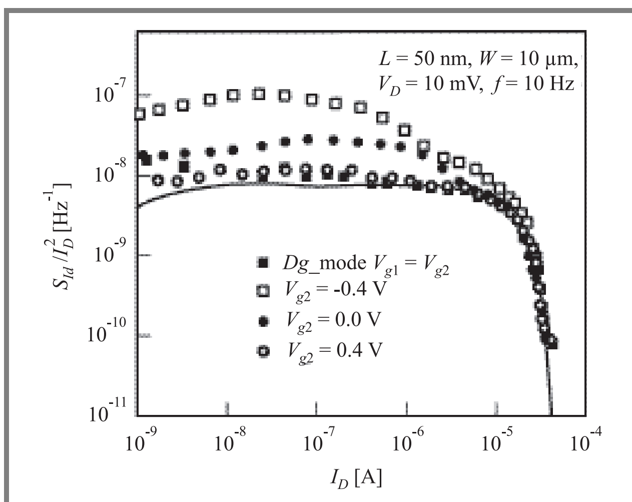

Fig. 7. Normalized drain current noise of a double gate NMOSFET for different back gate biases. Solid line: S_{VG} $(G_m/I_D)^2$ for double gate mode.

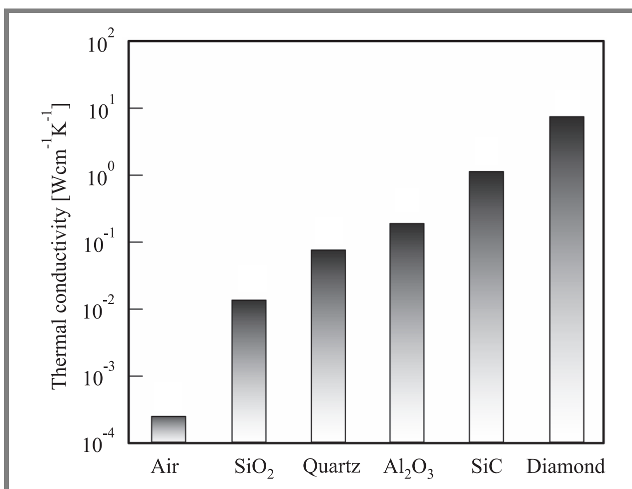

Fig. 8. Thermal conductivity of various buried oxide materials.

nel temperature and thus a reduction of carrier mobilities and drain current. The thermal conductance of various buried insulator materials is shown in Fig. 8 [8]. As it is shown in this figure, many insulators have a better thermal conductivity compared to SiO_2. In addition, diamond and quartz are also best suited dielectrics for controlling short channel effects and therefore to replace SiO_2. SiC and Al_2O_3 needs the use of thin buried insulator together with a ground plane architecture.

On the other hand, it is worth noting that the thermal conductivity of Ge films is lower than that of Si films for bulk materials (Fig. 9) [9]. However, for ultra-thin films,

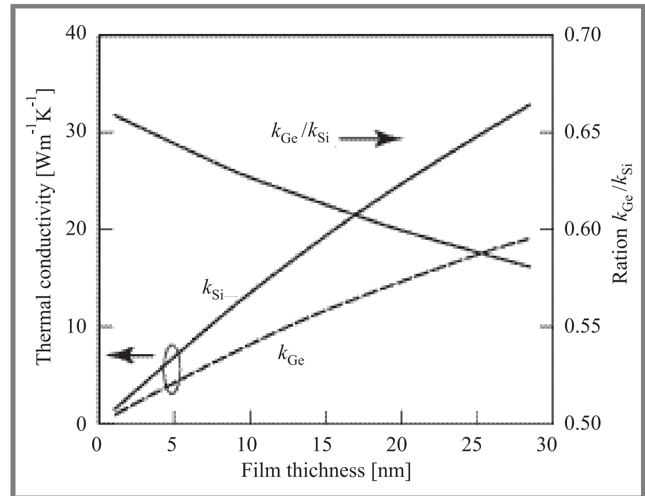

Fig. 9. Estimated thermal conductivity of thin Si and Ge layers.

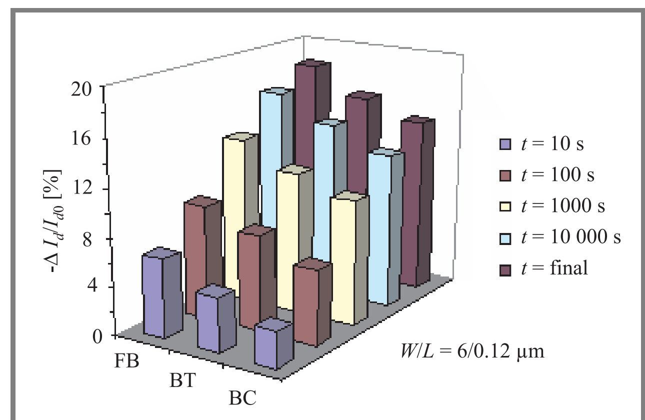

Fig. 10. Drain current degradation measured at $V_{GT} = 0.5$ V and $V_D = 50$ mV for various NMOSFET architectures in the worst-case aging scenario (aging conditions: $V_G = V_D = 2.2$ V).

these values are very close and therefore Ge films will present similar self-heating (SH) effects as Si films for deep sub-0.1 μm devices realized on nanometric layers.

Hot carrier effects are limiting long term device reliability. In SOI structures, special hot carrier regimes exist. Figure 10 shows the relative degradation of the drain current for various PD device architectures: floating body (FB), body connected (BC) and body tied (BT) [4]. This figure

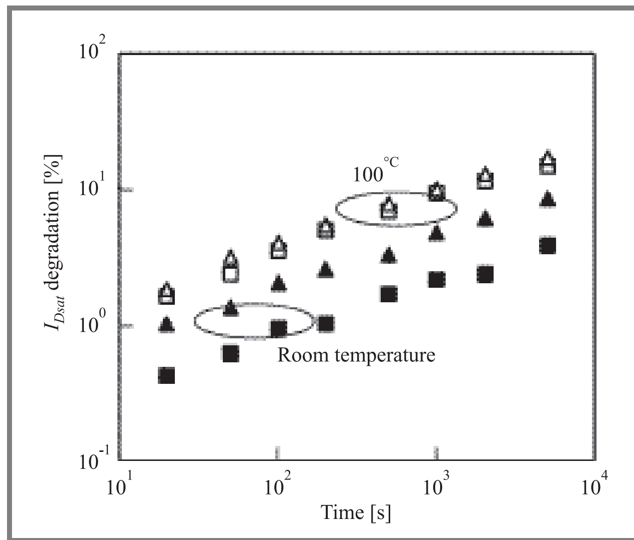

Fig. 11. Channel-width dependence of hot-carrier-induced degradation at room and high temperatures (squares – narrow, triangles – wide).

is plotted for the worst case aging in advanced SOI devices (maximum gate current, $V_G = V_D$). Body connected devices exhibit enhanced hot carrier immunity because of the collected hole coming from the impact ionization at the drain edge. Device degradation is also lowered for narrow channels due to reduced floating body effects (Fig. 11) [10].

3. Influence of strain and surface orientation on the electrical properties of thin layers on insulators

Compressive and tensile biaxial and uniaxial stress silicon technologies are promising for enhancing CMOS performance in bulk and SOI MOSFETs. The combination of strained layers and ultra thin films SOI structures is one of the best candidates for decananometer MOSFETs.

Figure 12 is a plot of the dependence of electron and hole mobilities as a function of the charge density [11]. The strained Si layer is fabricated with sacrificial thin relaxed SiGe and smart cut. In the SSOI devices, substantial enhancements of both electron (about 100%) and hole (about 50%) mobilities are obtained compared with the control SOI device at intermediate charge densities for long channel transistors.

An enhancement of the electron mobility of about 15–20% has been obtained for short channels (70 nm technology) SGOI MOSFETs (strained Si-on-SiGe-on-insulator) together with superior short channel control [12, 13]. Figure 13 shows the enhancement of the drain current for sub-0.1 μm devices.

In Fig. 14, the electron mobilities are represented for various Ge content of the SiGe layer and different Si film thicknesses. The electron mobility enhancement is max-

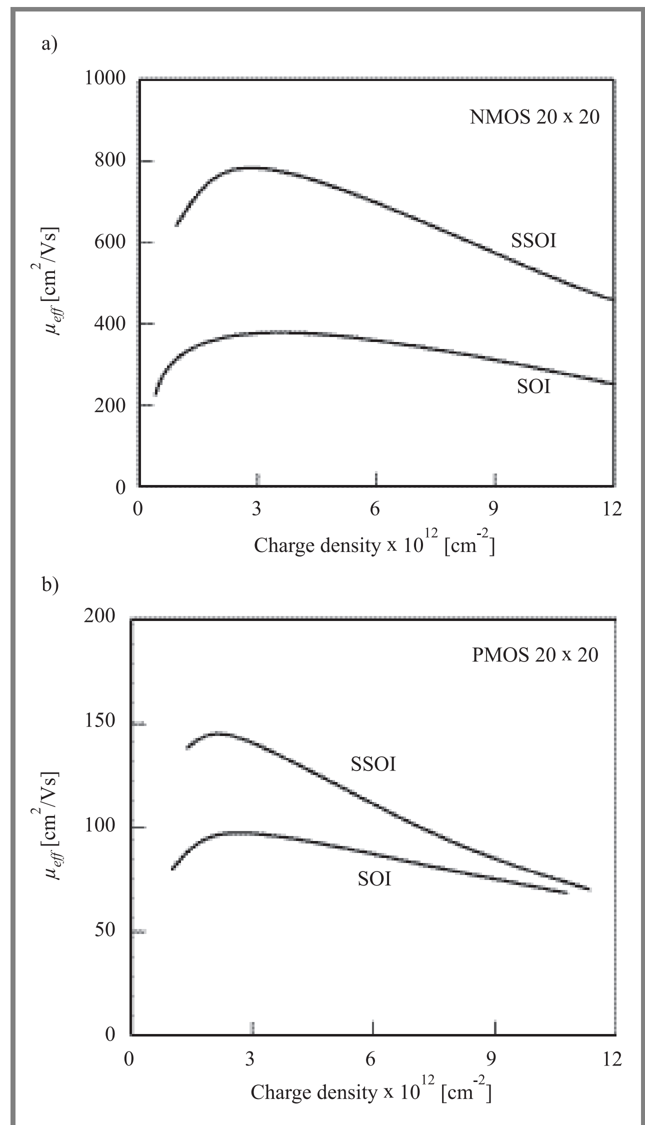

Fig. 12. Effective mobility comparison between SSOI and SOI MOSFETs: (a) electron mobility; (b) hole mobility.

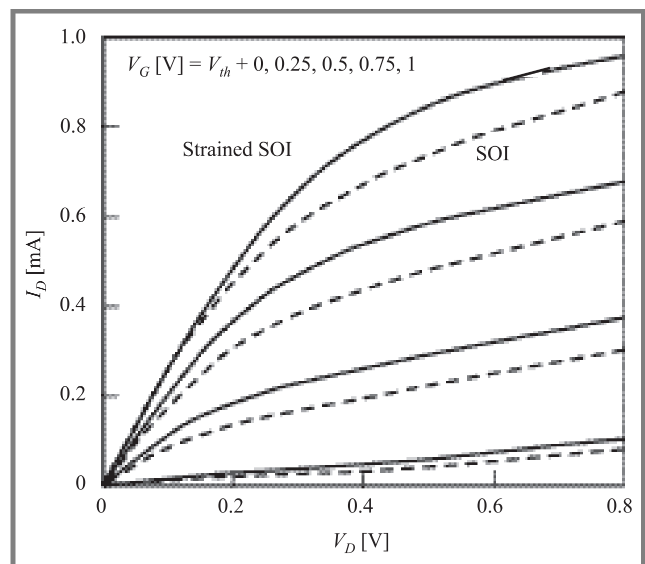

Fig. 13. I_D–V_D characteristics of 70 nm MOSFETs ($W = 1$ μm).

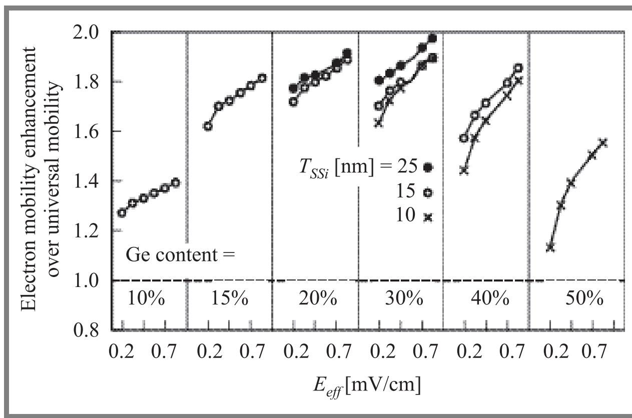

Fig. 14. Effective-field (E_{eff}) dependence of electron mobility enhancement as a function of Ge content and film thickness.

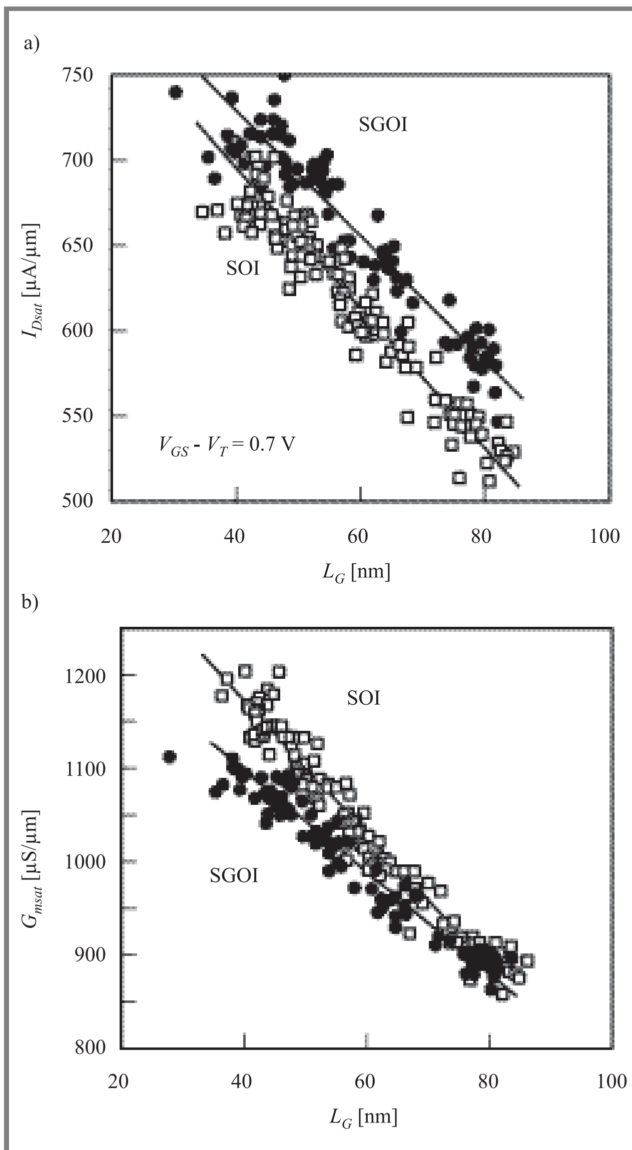

Fig. 15. Comparison of I_{Dsat} (a) and G_{msat} (b) at a constant gate overdrive.

imum for 30% of Ge due to the increase in alloy scattering and/or surface roughness for higher Ge concentrations and the hole mobility continuously increases with Ge up to 50% [13]. It is also worth noting that the enhancement of carrier mobility is reduced in thinner strained Si films due to interface states and fixed charges induced by the diffusion of Ge atoms to the interfaces.

Figure 15 shows I_{Dsat} and G_{msat} as a function of channel length for SGOI and SOI MOSFETs. An enhancement of I_D is outlined down to sub-50 nm transistors for SGOI, but the difference diminishes at smaller channel lengths due in particular to larger SH in SiGe than in Si. This SH effect in SGOI degrades G_{msat}, which is more sensitive to SH than I_D. Therefore the transconductance appears degraded in SGOI as compared to SOI but after correction of the self-heating a similar increase is obtained for I_D and G_m in the SGOI structure [14].

The HOI structure (strained Si/strained SiGe/ strained Si heterostructure-on-insulator) presents also substantial electron and hole mobility enhancements [15]. In particular, hole mobilities are very high for thin Si cap layer (enhancement of about 100%) compared with the universal SOI mobility and are also significantly higher that the best SSDOI mobility (strained Si directly-on-insulator) due to the compressively strained buried SiGe channel (Fig. 16).

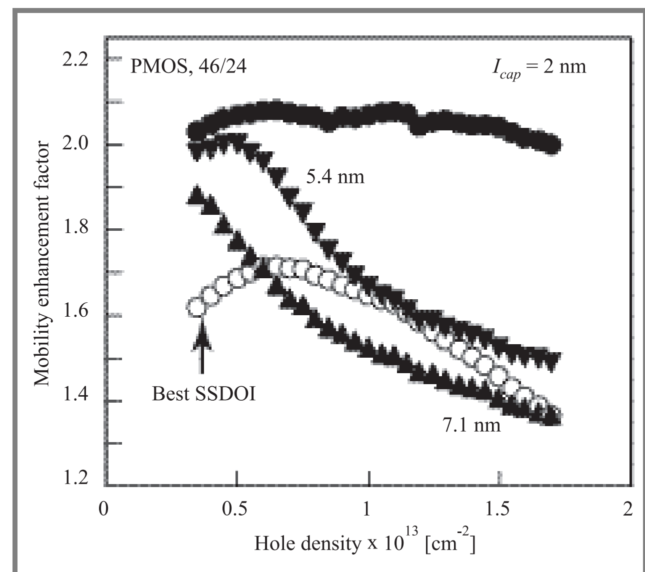

Fig. 16. Mobility enhancement in HOI compared with the best SSDOI curve relative to the universal SOI mobility.

Uniaxial strain engineering is also useful for mobility enhancement for Si film thickness in the sub-10 nm range [16]. A similar enhancement of electron mobility in 3.5 nm SOI devices under biaxial and uniaxial tensile strain has been obtained. The electron mobility is also enhanced in 2.3 nm Si layer under uniaxial tensile strain (Fig. 17), and the hole mobility increases in 2.5 nm film under uniaxial compressive strain.

It has recently been shown that the use of a metal gate (TiN) can induce significant compressive stress along the channel direction. This stress is increased as the gate length decreases. This phenomenon progressively degrades electron

mobility while hole transport is improved. Similar behaviors are obtained in single and double gate SOI devices, and the use of ⟨110⟩ channel orientation is the most favorable in terms of electrical performance [17].

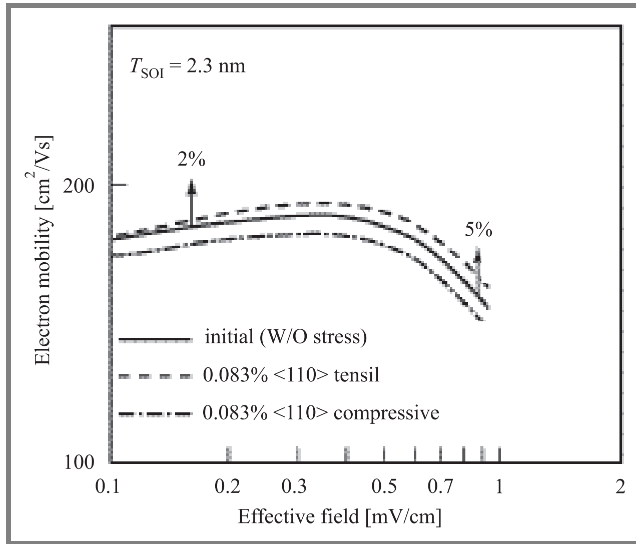

Fig. 17. Electron mobility in 2.3 nm ultra-thin-body MOSFET under ⟨110⟩ uniaxial strain.

Pure Ge channel MOSFETs are also considered as one promising option for future high performance CMOS. A compressively strained Ge channel is expected to further enhance hole mobility due to the very small effective

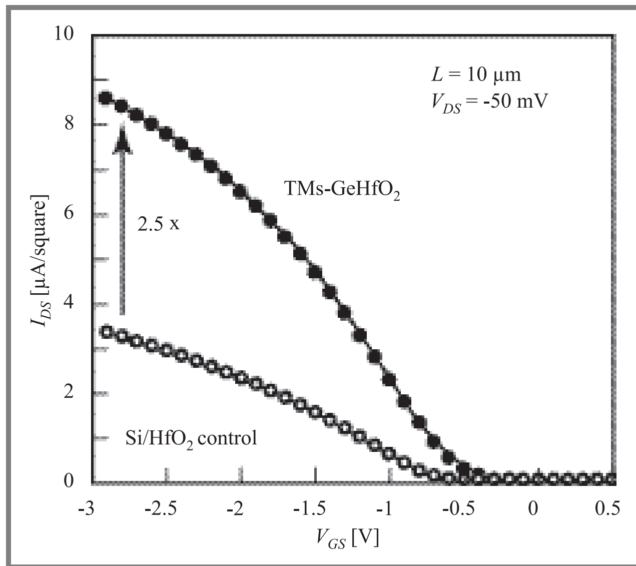

Fig. 18. Drain current of PMOSFETs with HfO_2 gate oxide on 60% Ge channel formed by local thermal mixing compared with Si PMOS control with HfO_2.

hole mass [18]. Figure 18 shows the linear current of s-Ge PMOS with HfO_2 gate dielectrics along with the Si control device. A 2.5 × performance enhancement is observed (similar enhancement for the transconductance). For s-Ge

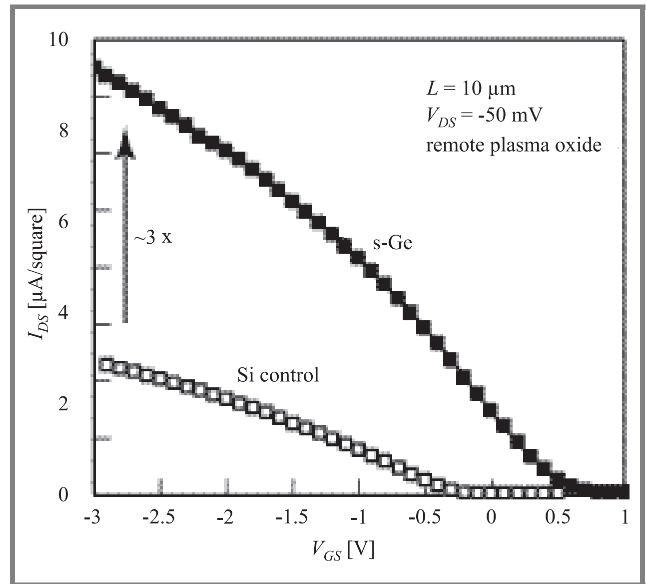

Fig. 19. Drain current of PMOSFETs with remote plasma oxide on 100% Ge channel formed by selective UHVCVD compared with Si channel PMOS control with the same oxide.

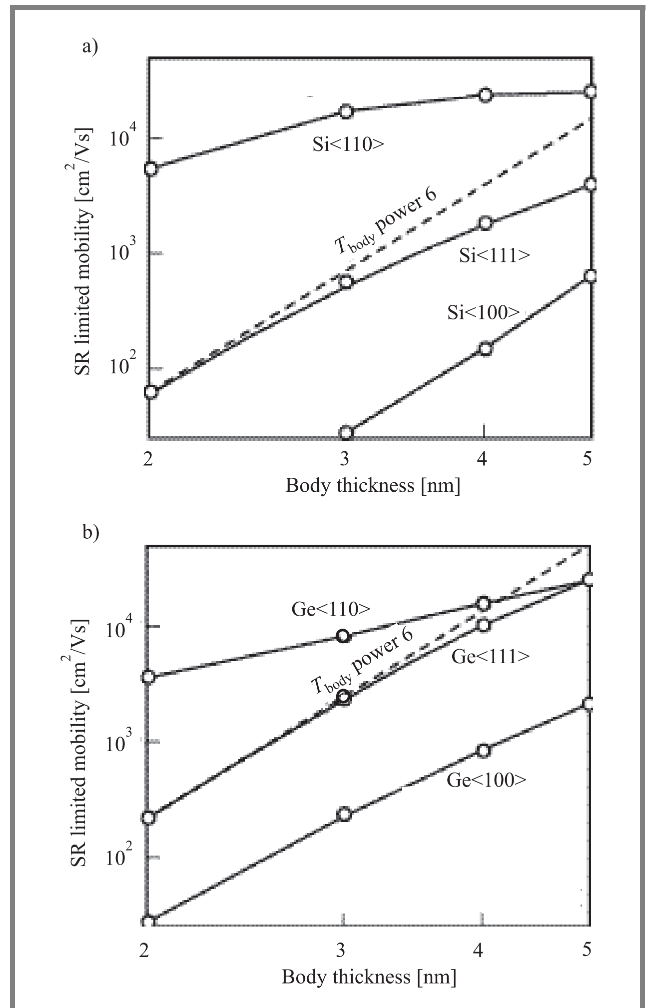

Fig. 20. Simulated surface-roughness limited hole mobility for Si (a) and Ge (b) with various orientations. Hole density $5 \cdot 10^{11}$ cm^{-2}.

P-type devices with SiO_2 gate oxide, a 3 × drive current and transconductance is obtained (Fig. 19).
The influence of surface-roughness (SR) in ultra-thin films is very important. Figure 20 shows the SR limited hole mobility as a function of body thickness for Si (SOI) and Ge (GOI) channels. The variation of hole mobility is outlined for various surface orientations [19].

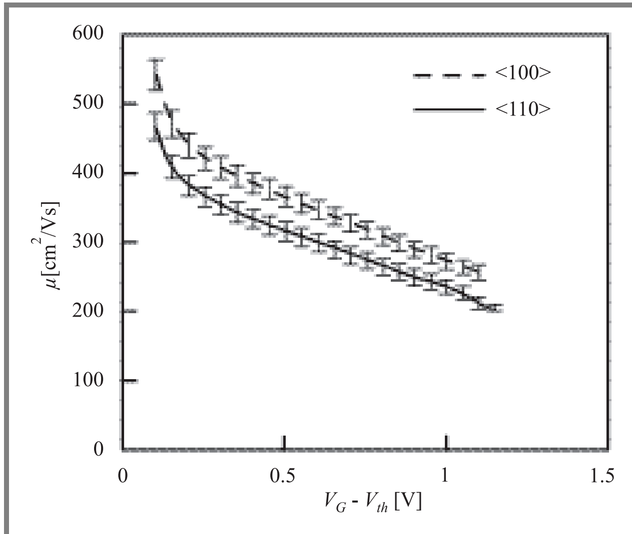

Fig. 21. Electron mobility of FinFETs with ⟨100⟩ and ⟨110⟩ fin orientation. $T_{ox} = 2$ nm, $4.5 \cdot 10^{13}$ cm^{-2} channel implantation.

Figure 21 represents electron mobilities in FinFETs with various fin orientations. An improvement of electron mobility is observed for ⟨100⟩ and an enhancement of hole mobility has also been shown for ⟨110⟩ orientation [20].

4. Comparison of the performance and physical mechanisms in multi-gate devices

Multi-gate MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion in the conductive layer [21].
The on-current I_{on} of the MOSFET is limited to a maximum value I_{BL} that is reached in the ballistic transport regime. Figure 22 reports the self-consistent Monte Carlo (MC) simulation of the ballistic ratio $BR = I_{on}/I_{BL}$ versus drain induced barrier lowering (*DIBL*) showing that one can increase the *BR* by scaling the gate length, thus increasing the longitudinal field at the source, but this comes at the cost of a larger *DIBL*. For a given *DIBL*, an increased ballisticity is obtained for low doping double gate SOI devices [22].
The transfer characteristics of several multiple-gate (1, 2, 3 and 4 gates) MOSFETs, calculated using the 3D Schrödinger-Poisson equation and the non-equilibrium Green's function formalism for the ballistic transport or MC simulations, have shown similar trends. The best performance (drain current, subthreshold swing) is outlined for the 4-gate (QG or GAA) structure [23, 24] (Fig. 23).

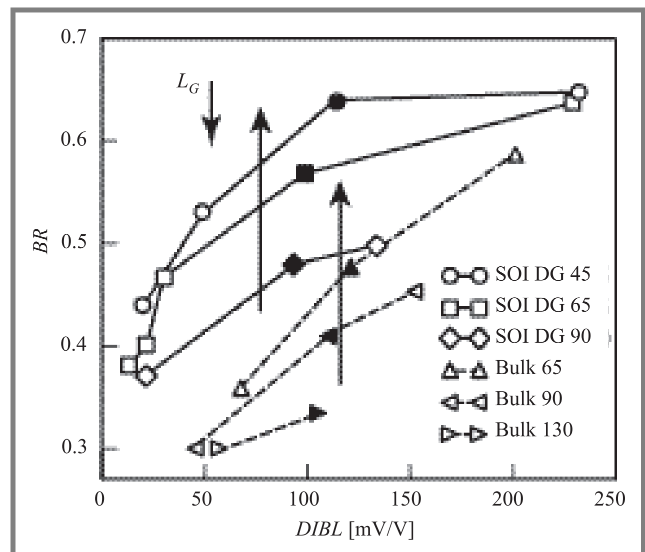

Fig. 22. Ballisticity ratio at $V_G = V_D = V_{DD}$ versus *DIBL*. Filled symbols represent transistors with the nominal gate length for the high-performance MOSFET of each technology node.

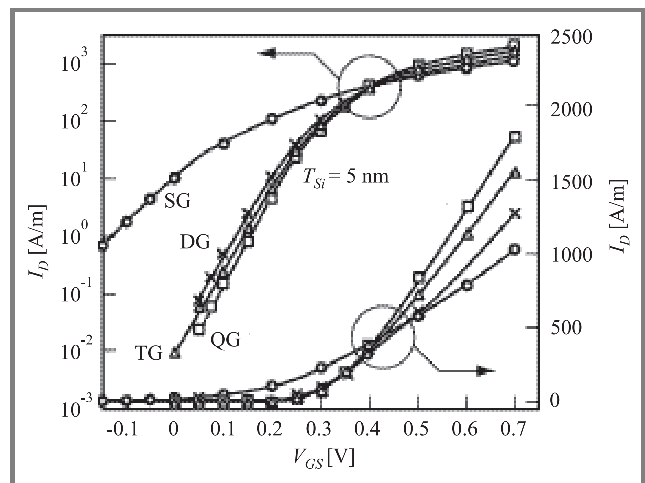

Fig. 23. I_D–V_{GS} characteristics at $V_{DS} = 0.7$ V in thin layers for different multi-gate architectures.

However, Fig. 24 demonstrates that the propagation delay in triple gate (TG) and quadruple gate (QG) MOSFETs are degraded due to a strong rise of the gate capacitance. A properly designed double-gate (DG) structure appears to be the best compromise at given I_{off} [24].
Figure 25 compares the calculated ballistic drive current for Si and Ge double-gate MOSFETs at the operation point of each generation as predicted by International Technology Roadmap for Semiconductors (ITRS) [25]. Si barely satisfies the ITRS requirement, whereas Ge offers much higher current drive. However, the simulated value of the real drain current of 2G SOI transistors is not able to satisfy the ITRS objectives, even for intrinsic devices without

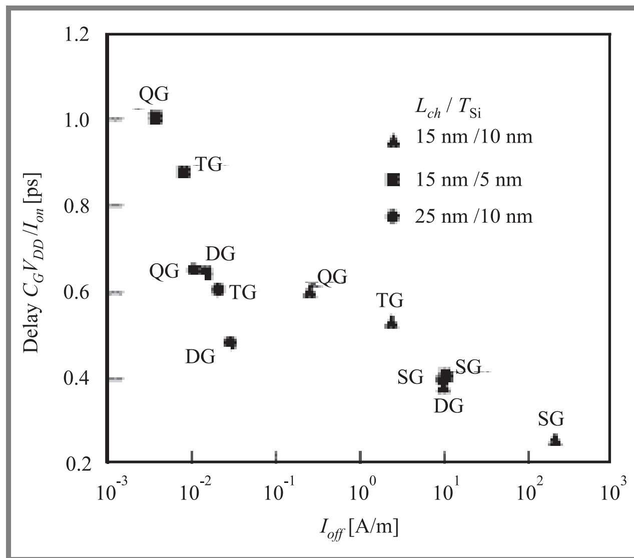

Fig. 24. Propagation delay versus I_{off} for single-gate and multi-gate SOI devices.

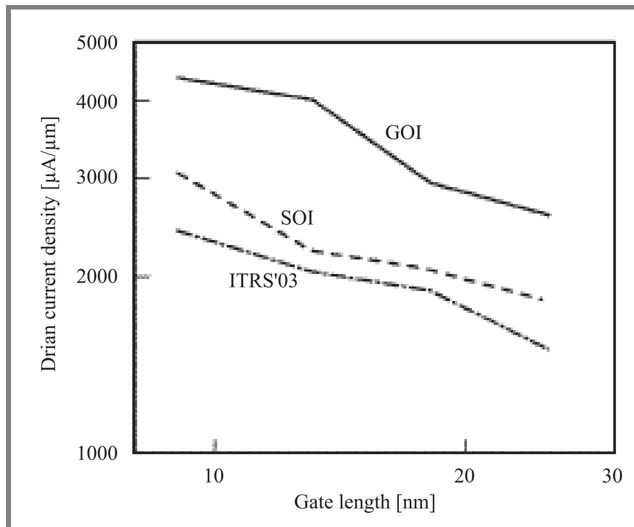

Fig. 25. Ballistic drive current for different technology nodes for SOI and GOI devices.

parasitic S/D resistances. The 2G GOI MOSFETs are able to provide the needed current drive, but parasitic resistances drastically affect the drain current (not shown here).

For a double gate device, the impact of a gate misalignment on the leakage current is important. This current is mainly due to gate induced leakage current (GIDL). This off-current is enhanced with increasing the misalignment and it is higher for a shift of the bottom gate towards the drain due to a higher V_{GD} compared to V_{GS} [26].

The impact of a gate misalignment is also significant for I_{on} in 2G MOSFETs [27]. A large back gate (BG) shift reduces the saturation current compared to the aligned case, whereas a slight BG shift towards the source increases I_{on}. This is due to a lower source access resistance. In terms of short channel effects, aligned transistors exhibit the best control while highly misaligned MOSFETs operate like single gate ones. The off-current I_{off} is much more influenced by the misalignment than I_{on} due to a degradation of the electrostatic control (Fig. 26). The oversized transistor shows attractive static performance (right hand side of Fig. 26) and a better tolerance to misalignment but the dynamic performance is rapidly degraded as the overlap length increases.

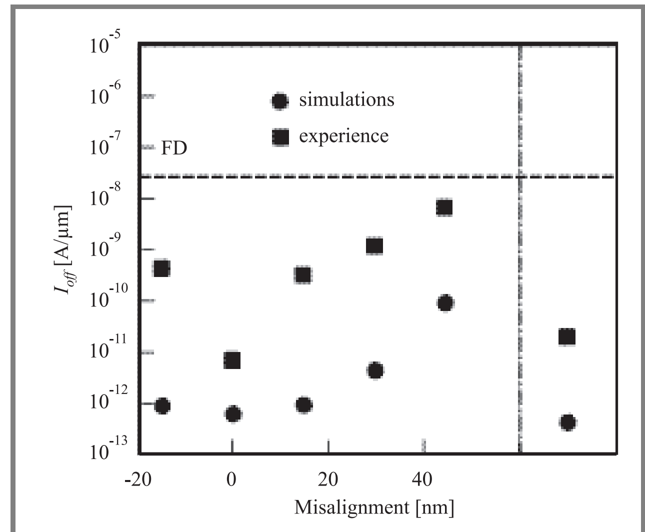

Fig. 26. Evolution of I_{off} with misalignment (experimental and simulations results, $V_D = 1.2$ V). Single gate FD results are represented by a dashed line.

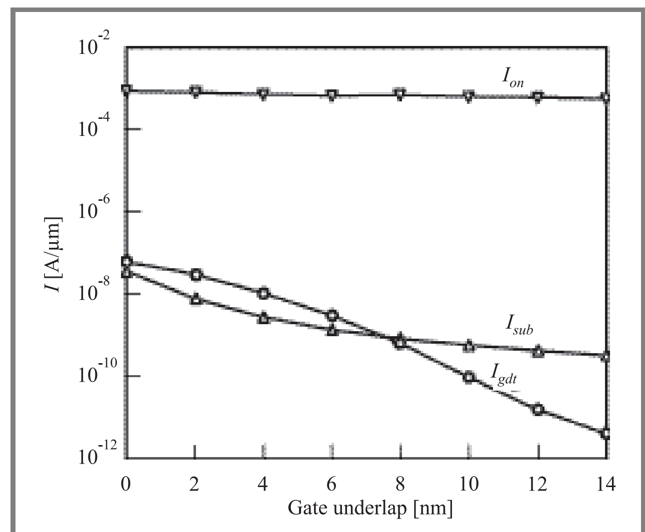

Fig. 27. I_{on}, subthreshold (I_{sub}) and gate direct tunneling (I_{gdt}) currents as a function of gate underlap.

In decananometer MOSFETs, gate underlap is a promising solution in order to reduce the *DIBL* effect. Figure 27 presents the variations of the driving current, the subthreshold current and the gate direct tunneling current versus gate underlap [28]. The on-current is almost not affected by

the gate underlap whereas the leakage currents are substantially reduced due to a decrease in DIBL and drain to gate tunneling current. A reduction of the effective gate capacitance C_G for larger underlap values at iso I_{on} has also been shown. This reduction of C_G leads to a decrease in the propagation delay and power.
Multi-bridge-channel MOSFETs (MBCFET) also present very high performance better than that of gate-all-around (GAA) devices and exceeding the ITRS roadmap requirements (Fig. 28) [29].

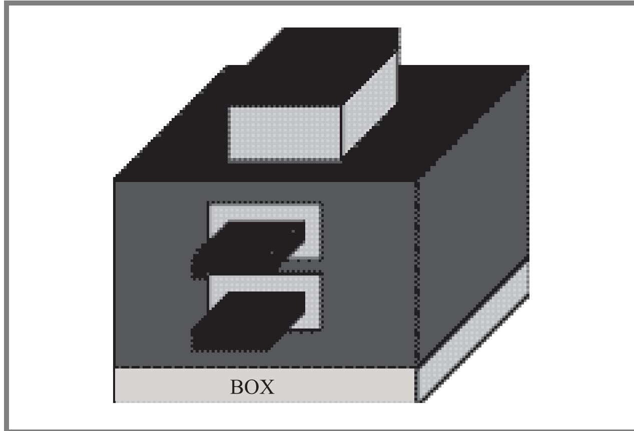

Fig. 28. Schematic diagram of MBCFET on SOI.

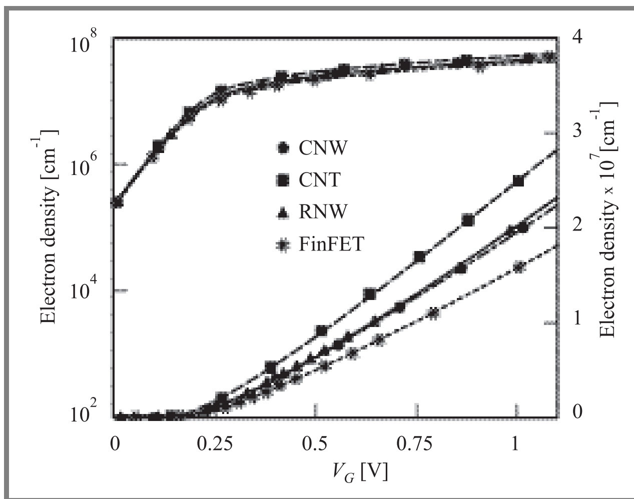

Fig. 29. Electron density per unit length for various devices (FinFET, nanowires and carbon-nanotube FET). 65 nm technology node data (EOT = 0.9 nm, $T_{Si} = 5$ nm).

Finally, FinFETs are compared with cylindrical (CNW) and rectangular (RNW) nanowires and also with gate-all-around carbon nanotubes (CNT) FET. It is shown that the CNTFET exhibits superior performance (Fig. 29) due to electron charge confinement at the surface of the nanotube, whereas in the Si-based nanowires the charge confinement at the center of the wire is responsible for an additional depletion capacitance in series with the oxide capacitance, which reduces the overall effectiveness of the gate [30].

5. Advanced SOI dynamic and non-volatile RAM

It is becoming difficult for memories to be scaled down. Indeed, traditional embedded dynamic random-access memory (DRAM) requires a complicated stack capacitor or a deep trench capacitor in order to obtain a sufficient storage capacitance in smaller cells. This leads to more process steps and thus less process compatibility with logic devices.
Capacitor-less 1T-DRAM or floating body cells have shown promising results. The operation principle is based on excess holes which can be generated either by impact ionization or by gate-induced leakage current in partially-depleted SOI MOSFETs. The GIDL current is due to band-to-band tunneling and occurs in accumulation leading to a low drain current writing and reduced power consumption together with a high speed operation. However, conventional PD SOI MOSFETs require high channel doping to suppress short-channel effects, which induces a degradation in retention characteristics. In order to overcome this problem, a DG-FinDRAM has been proposed showing superior memory characteristics (Fig. 30) [31].
Conventional floating-gate flash memory has also scaling difficulties due to nonscaling of gate-insulator stack and inefficient hot carrier injection processes at sub-50 nm gate

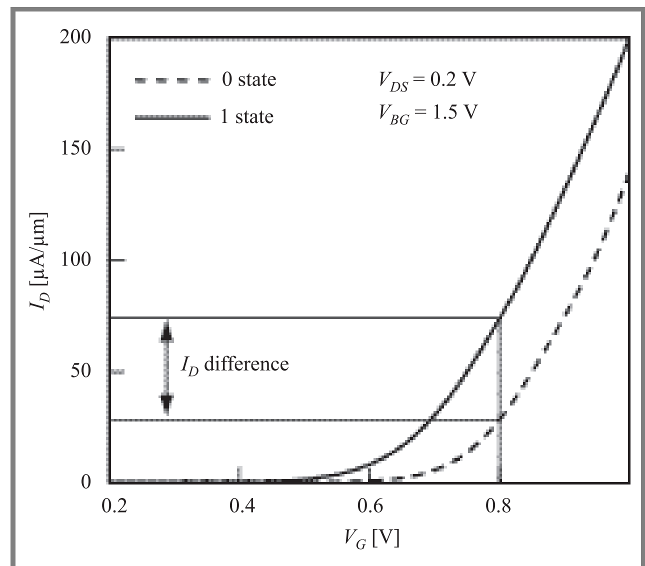

Fig. 30. I_D–V_G characteristics of the DG-FinDRAM.

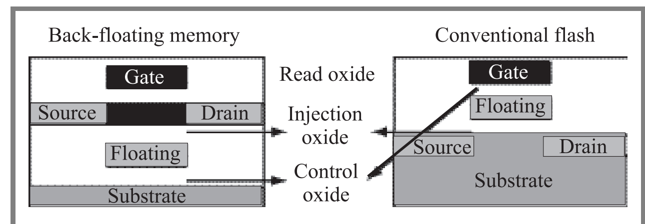

Fig. 31. Cross-sections of back floating gate and conventional front-floating gate memories.

dimensions. Back-floating gate flash memory overcomes these limitations by decoupling read and write operations and independent positioning and/or sizing of the storage element (back-floating gate) under the Si channel (Fig. 31). The charge in the back gate affects the field and the potential at the bottom interface and thus changes the threshold voltage of the device. The back-floating gate is charged by applying –10 V to the source, the drain and the front gate simultaneously, and the charges are removed from the back floating gate (erasing) with the same method but with a bias of +10 V [32].

6. Conclusion

In this paper, a review of recently explored new effects in advanced SOI devices and materials has been given. The impact of key device parameters on electrical and thermal floating body effects has been addressed for various device architectures. Recent advances in the understanding of the sensitivity of electron and hole transport to the tensile or compressive uniaxial and biaxial strains in thin film SOI have been shown. The performance and physical mechanisms have also been presented in multi-gate MOSFETs. New hot carrier phenomena have been discussed. The impact of gate misalignment or underlap, as well as the use of the back gate for charge storage in double-gate nanodevices and of capacitorless DRAM have also been outlined.

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