Invited paper

On-wafer wideband characterization: a powerful tool for improving the IC technologies

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Abstract— In the present paper, the interest of wideband characterization for the development of integrated technologies is highlighted through several advanced devices, such as 120 nm partially depleted (PD) silicon-on-insulator (SOI) MOSFETs, 120 nm dynamic threshold (DT) voltage – SOI MOSFETs, 50 nm FinFETs as well as long-channel planar double gate (DG) MOSFETs.

Keywords—silicon-on-insulator, MOSFET, wideband characterization, microwave frequency, extraction techniques, small-signal equivalent circuit.

1. Introduction

Usually, at the early stage of advanced transistor development only the static behavior of novel devices is considered. Indeed, the I_{on}/I_{off} ratio, the subthreshold slope (S), the threshold voltage roll-off and the drain induced barrier lowering (DIBL) are the primary figures of merit that are extracted after each process run and which provide insights into the process quality.

The static analysis of the built transistors is then extended to the measurements of the gate transconductance (G_m) in saturation as well as the output conductance (G_d) or early voltage (V_{EA}). A typical feature of a node development scheme is that the dynamic behavior of advanced devices is most of the time considered only at the end of the fabrication process developments. Moreover, this dynamic analysis is usually limited to the frequency band of available vectorial network analyzer (VNA) leading to an unexplored frequency band beginning somewhere between a few Hz and 1 GHz.

However, a full frequency band analysis is precious for separating physical phenomena taking place in advanced MOS devices and characterized by clearly distinct time constants. Indeed, thermal and floating body effects typically appear from DC up to a few kHz in partially depleted (PD) SOI devices. In the MHz range the efficiency of the body contact in body-contacted (BC) PD SOI MOSFETs starts to degrade and untied carriers (i.e., minority carriers in the substrate or majority carriers in a floating body) can no longer follow the AC excitation. Finally, in the GHz range the relaxation time related to majority carriers is no more negligible and most of the parasitic capacitances and resistances specific to the 3D physical structure mainly affect the dynamic behavior of active devices.

Electrical characterization between DC and 110 GHz of advanced SOI MOS devices will be presented in this paper. Several direct characterization techniques have been developed for extracting small and large signal electrical models. Beside measurement facilities, our laboratory has several commercially available simulation software. We have already successfully simulated DC and RF behavior of MOSFETs such as fully and partially depleted, body-contacted and dynamic threshold MOSFETs in SOI technology. The 3D module of Atlas was used for simulating gate-all-around MOS as well as FinFETs. Combining the experimental characterization techniques and the simulation facilities, we have developed several macro-models based on a complete extrinsic small-signal equivalent circuit and an improved CAD model for the intrinsic device for those types of SOI MOSFETs.

2. Gate induced floating body effects in ultrathin oxide PD SOI MOSFET

Tunneling through gate oxides about 2-nm-thick is one of the major challenges faced by today's bulk-Si and SOI CMOS technologies. Gate tunneling does not only increase device leakage and power dissipation, but also leads to charging and discharging of PD SOI MOSFET body region causing floating body and device history-dependent effects [1, 2]. For n-type PD SOI MOSFETs, gate tunneling injects holes into the floating body thus increasing its voltage. This affects the device DC-characteristics and induces the so-called gate induced floating body effects (GIFBE) recently disclosed in [3, 4]. The impact of GIFBE on device DC transconductance was carefully examined in [3, 4], in which it was shown that gate tunneling induces a sharp second peak in the G_m-gate voltage curve of the studied devices. It was also demonstrated that the amplitude as well as the location of this peak are dependent on the measurement conditions and the device history.

Recently, we proposed a method based on wideband small-signal frequency measurements to characterize the dynamics of GIFBE [5]. This study was performed on n-channel 120 nm PD SOI MOSFETs with a silicon film and a buried oxide thickness of respectively 150 and 400 nm and a gate oxide with the thickness of approximately 2 nm. The DC measurements were performed with an HP4145 at

a drain bias of 50 mV and using a delay time of 2 s between successive DC points. The results of the DC measurements clearly display GIFBE (Fig. 1), since a second peak appears in the G_m versus V_g curve. This peak is associated with a DC body voltage increase caused by the injection of holes, which are generated by electron valence band tunneling through the gate oxide [3, 4]. The experimental set up used for the AC measurements is depicted in the inset of Fig. 1. A small amplitude (20 mV) AC signal at the gate electrode was superimposed on the DC bias using an HP3563 system analyzer. The AC variations of the drain current were recorded by measuring the potential drop across a resistance and an operational amplifier was also used to fix the DC drain bias at 50 mV. The AC measurements were performed between 0.1 Hz and 10 kHz for various DC bias conditions. The AC values are displayed in Fig. 1 for different frequencies.

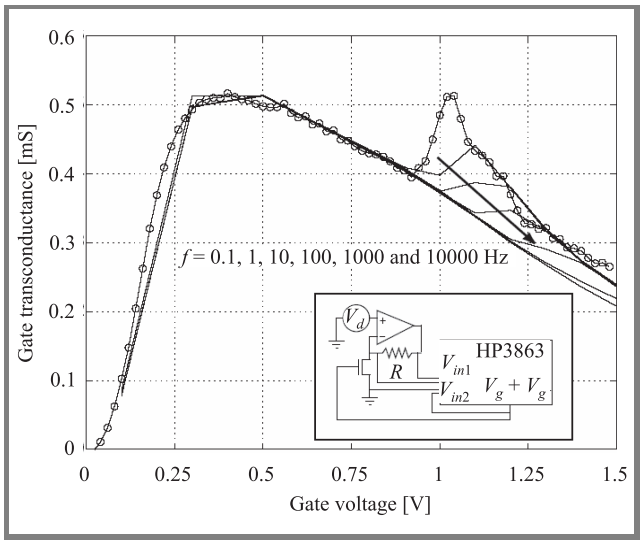

Fig. 1. Total gate transconductance G_m versus gate voltage for a floating body PD SOI MOSFET with $L = 2$ μm, $W = 60$ μm and $V_d = 50$ mV.

These AC variations of G_m are expected to have negative impact on low-frequency analog circuits requiring high gain and high accuracy. For example, in the case of operational amplifiers, they may cause gain reduction at very low frequencies and produce circuit instabilities due to reduced settling time constants.

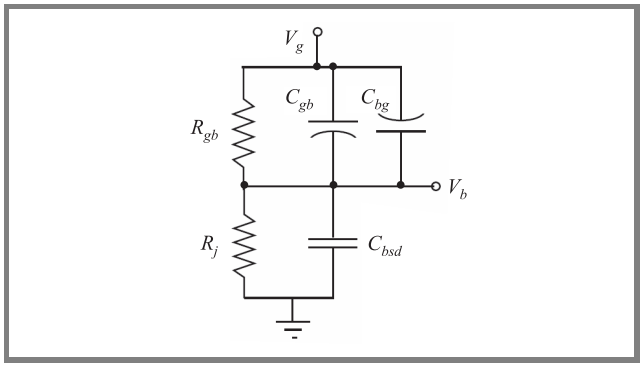

Fig. 2. Equivalent circuit of internal body node dynamic behavior due to AC gate excitation through ultrathin gate oxide for a floating body PD SOI MOSFET.

As shown in details in [5] GIFBE are characterized by a very low frequency pole that is associated with the high impedance seen by the floating body toward external nodes. These effects can be relatively well reproduced with the BSIMSOI [11] model and with a simple equivalent AC circuit that includes the internal body node as well as gate tunneling (Fig. 2).

3. High frequency degradation of body-contacted PD SOI MOSFET output conductance

Partially depleted SOI technology suffers from non linearities in MOSFET output conductance introduced by the so called "kink effect". Under DC or low frequency conditions, this inconvenience has now been successfully overcome by several alternative solutions, such as fully depleted (FD), body tied (BT) or dynamic threshold (DT) MOS devices (Fig. 3) [6]. However, with the aggressive downscaling of channel length and SOI film thickness the efficiency of the body contact is reduced due to an increase of body resistance. In [7, 8], we analyzed the efficiency of the body contact from an output conductance point of view by comparing the G_d values measured on floating body (FB), BT, DT and FD devices of the 0.18 and 0.24 μm SOI technology node. The measurements were performed in DC and in the 100 kHz – 4 GHz frequency range.

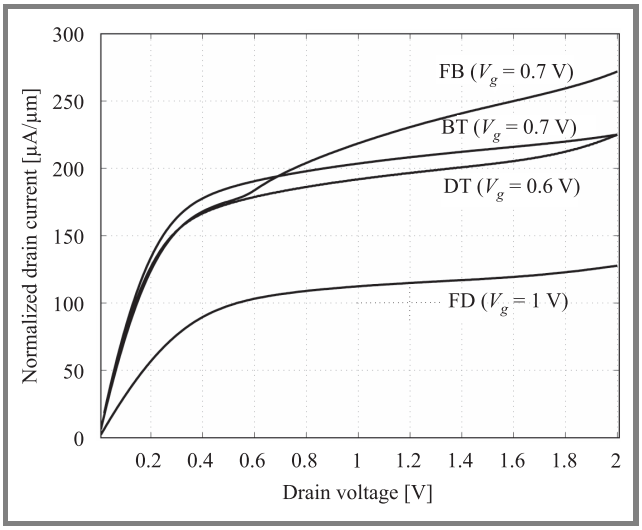

Fig. 3. Measured drain current I_d normalized by the total drawn gate width for FB, BT, DT PD SOI MOSFETs with $L = 0.18$ μm and FD SOI MOSFET $L = 0.24$ μm.

At low frequencies, Fig. 4 highlights the significant improvement obtained on G_d by connecting the body to the source or the gate, since both DT and BT structures exhibit a value of G_d more than two times lower than that of FB devices. However, it seems that this positive effect is lost at higher frequencies, since both DT and BT devices suffer from a 150% G_d degradation between DC and high frequency (4 GHz) levels.

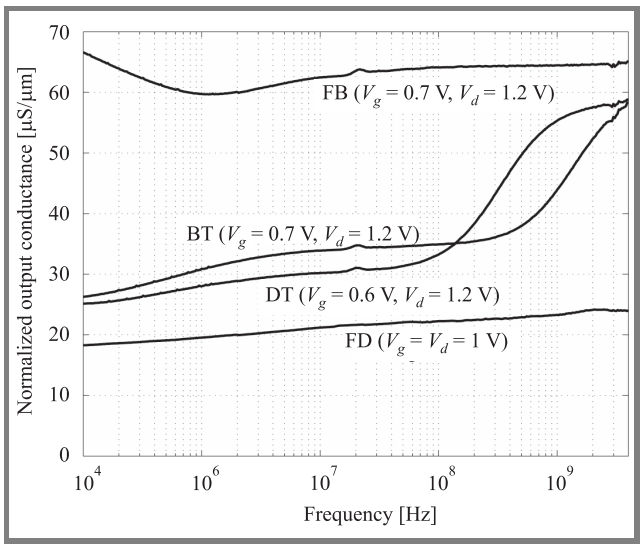

Fig. 4. Normalized output conductance measured as a function of the frequency for the different devices under analysis.

To explain and discuss these observations we proposed in [7, 8] small signal modeling of the PD devices seen from the drain terminal. The model includes the body region and its accesses to external nodes. It also accounts for AC impact ionization effects and AC charging of body potential. The model clearly points to the non zero value of the body resistance (R_{be}) as the origin of the G_d degradation. Reducing R_{be} by technological means would then provide an efficient way to reject this parasitic G_d increase to higher frequencies. In the next section an original method based on 3-port RF measurements [9] to accurately extract the body resistance in body-accessed PD SOI MOSFETs is presented.

4. Extraction of the body contact resistance

Accurate characterization of R_{be} is crucial to assess the efficiency of the body contact in a given technology. It can also be used to assess the validity of compact models such as BSIMSOI. The proposed method is based on the measurement of S-parameters over a wide frequency band under three-port configuration: the two classical ports are for the gate and the drain and the third port is connected to the body of the device.

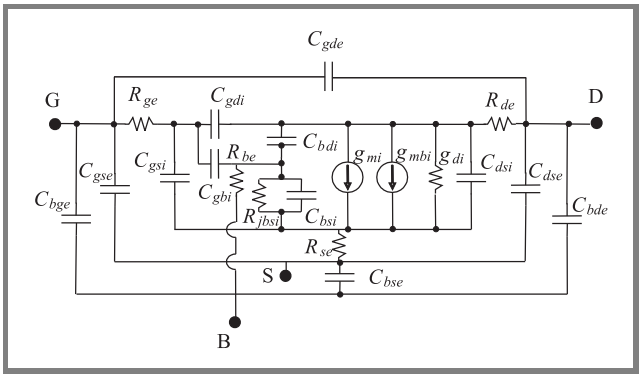

Fig. 5. Complete small signal equivalent circuit of the 3-port devices, including the external body node.

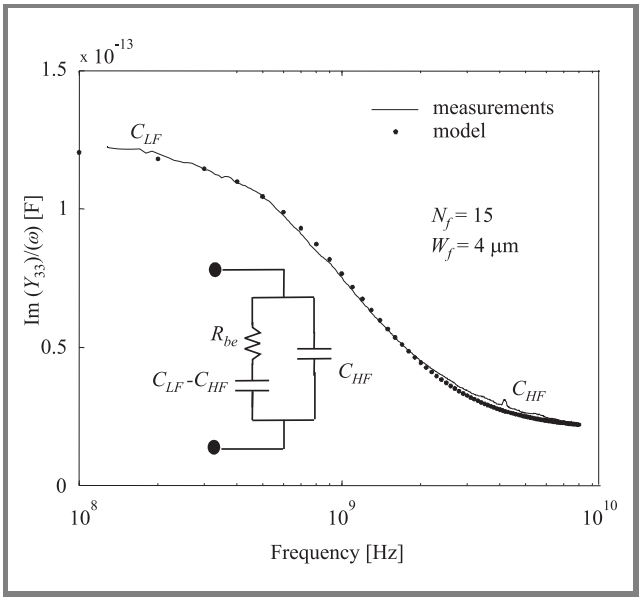

Fig. 6. Measured and simulated $\mathrm{Im}(Y_{33})/(\omega)$ data as a function of frequency for $V_g = V_b = 0.6$ V and $V_d = 1.2$ V, inset: R-C model used.

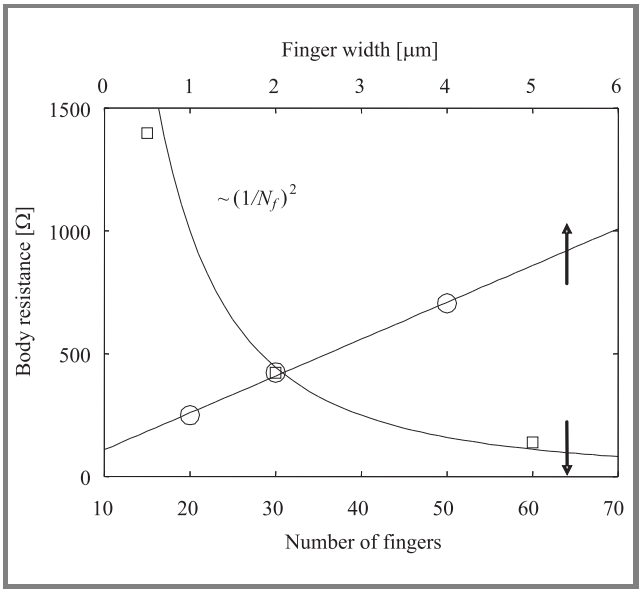

Fig. 7. Extracted values of R_{be} with respect to W_f and N_f.

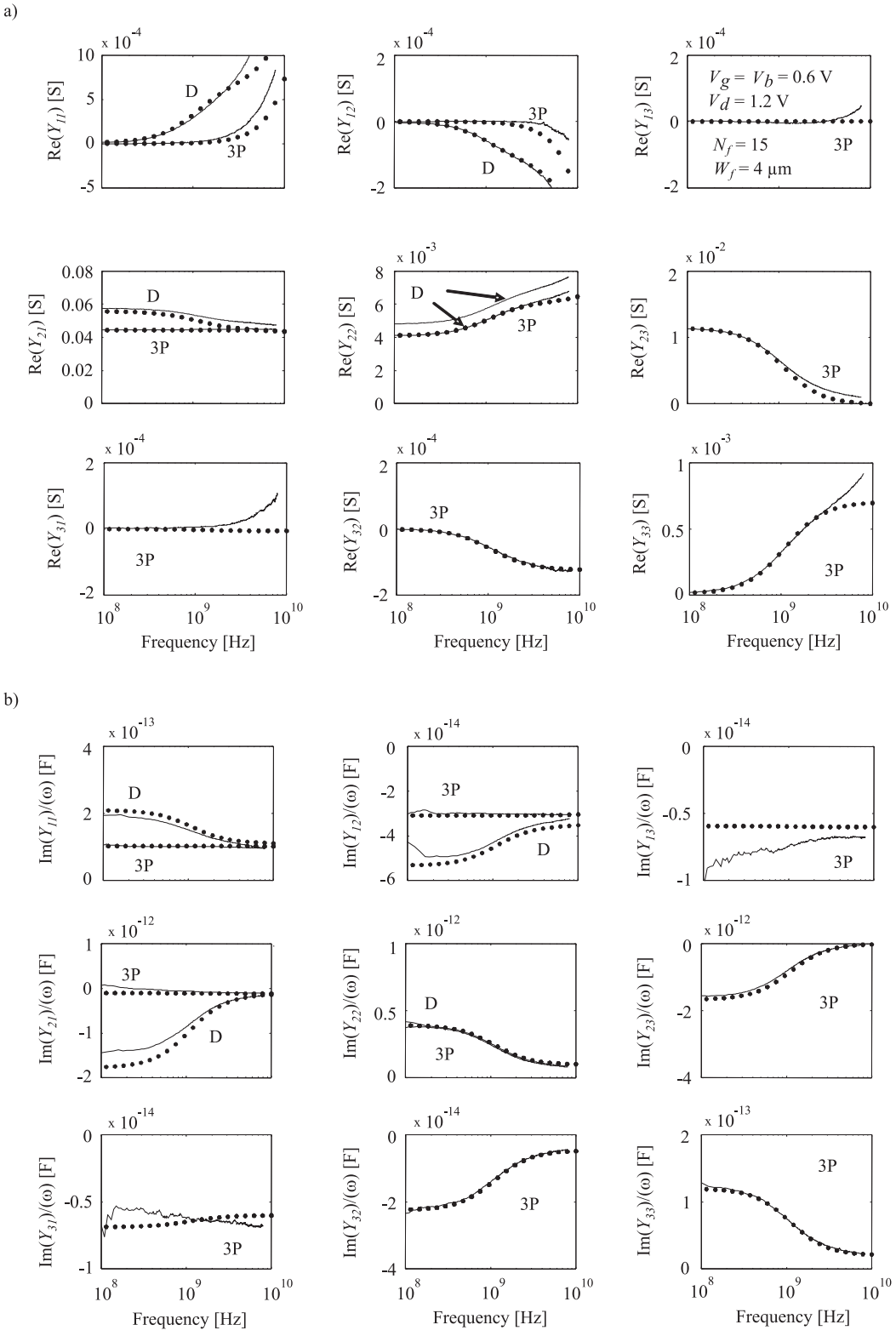

Fig. 8. Measured (straight lines) and simulated (dots) (a) $\mathrm{Re}(Y_{ij})$ and (b) $\mathrm{Im}(Y_{ij})/(\omega)$ for the 3-port device (3P) as well as for the DTMOSFET with body connected to gate.

The measured devices originate from a 0.13 μm SOI technology from ST Microelectronics, Grenoble. Different geometries (varying number of fingers (N_f) or finger width (W_f)) and body connections (either to the gate (DT) or to a third RF access) were considered. In all cases the body was accessed at both sides of the active area in order to reduce R_{be}. The S-parameters were measured with a multiport Rhode&Schwartz VNA up to 8 GHz and were de-embedded with a 3-port open subtraction method.

The modeling of the RF PD SOI devices was based on the small signal equivalent circuit presented in Fig. 5. It can be seen that both intrinsic (subscript i) and extrinsic (subscript e) elements were considered between each pair of electrodes, including the body (B). By extrinsic, the authors mean all parasitics that could not be removed during the de-embedding step.

The modeling of the body node was therefore achieved by considering all extrinsisic capacitances (C_{bge}, C_{bse} and C_{bde}), its access resistance (R_{be}), its intrinsic body-gate (C_{bgi}) as well as body-source (C_{bsi}) and body-drain (C_{bdi}) junction capacitances, and its intrinsic body-source junction resistance (R_{jbsi}). The body-drain junction resistance was neglected due to reverse biasing of this junction when devices operate in saturation. The extraction of R_{be} was performed by analyzing the output admittance seen from the body node terminal (Y_{33}). Indeed, as shown in Fig. 6 the value of $\mathrm{Im}(Y_{33})/(2\pi f)$ clearly exhibits a pole-zero pair dependence, which is typical of the simple R-C network included in Fig. 6. In this circuit, the high frequency (C_{HF}) value of $\mathrm{Im}(Y_{33}/(2\pi f)$ is simply the sum of all extrinsic capacitances seen from the body terminal (i.e., $C_{HF} = C_{be} = C_{bse} + C_{bde} + C_{bge}$) while its low frequency value (C_{LF}) is the sum of all intrinsic and extrinsic capacitances seen from the body terminal (i.e., $C_{LF} = C_{bsi} + C_{bdi} + C_{bgi} + C_{be}$). In these conditions, it is immediate to see that the pole expression is given by

$$f_p = \frac{1}{2\pi R_{be}(C_{LF} - C_{HF})} = \frac{1}{2\pi R_{be}(C_{bsi} + C_{bgi} + C_{bdi})} \quad (1)$$

and is therefore strongly dependent on the value of R_{be}.

By fitting the R-C network to the measurement results this value could then be extracted. Figure 7 shows the value of R_{be} obtained for devices with varying N_f (with constant $N_f W_f$ product) and W_f (with constant N_f) values. It is seen that Eq. (1) R_{be} decreases approximately as $(1/N_f)^2$ (similarly to R_{ge} [10]) while Eq. (2) a linear dependence on W_f is observed. These two trends agree with predictions made by the scalable BSIMSOI model [11], further supporting the validity of the extraction method.

The extrapolated value of R_{be} obtained for $W_f = 0$ ($\sim$150 Ω) therefore provides a good estimation of the parasitic resistance associated with the body interconnects (R_{bout}) outside the active region. The figure shows that its contribution is not negligible with regards to the overall value of R_{be}. Indeed, normalized values of R_{be} and R_{bout} were found to be close to 21 kΩ/μm $\cdot$ finger and 2.25 k$\Omega \cdot$ finger, respectively, assuming only one contact per finger. The body node characterization was further achieved by extracting (C_{bge}, C_{bgi}) and (C_{bde}, C_{bdi}) from the high frequency and low frequency parts of $\mathrm{Im}(Y_{31})$ and $\mathrm{Im}(Y_{32})$, respectively. The body-source capacitances were then obtained from C_{LF} and C_{HF} and the back gate transconductance (g_{mbi}) was given by $\mathrm{Re}(Y_{23})$. The value of R_{jbsi} could theoretically be extracted from $\mathrm{Re}(Y_{33}) = (R_{be} + R_{jbsi})^{-1}$ at low frequencies but was too high ($>$ 100 kΩ) to be accurately measured. It was therefore assumed to be infinitely high in the model. The rest of the device parameters were obtained with the Cold-FET method [10], while R_{se}, R_{de} and R_{ge} were obtained with a method depicted in [12]. Figures 8a and 8b show that an accurate modeling of both real and imaginary parts of the Y parameters is obtained up to $\sim$ 4 GHz for a 4 μm-wide device with $N_f = 15$, $V_g = 0.6$ V, $V_d = 1.2$ V, $V_b = 0.6$ V. The model was then further tested by connecting the body to the gate terminal, forming a two-port network and compared with measurement results obtained on a DTMOSFET with the same geometry. It is seen in Figs. 8a and 8b that a good agreement is obtained between measured and simulated data, despite a small output conductance difference observed for the DTMOSFET, which could be due to a subtle bias shift.

5. Extraction of parasitic capacitances and resistances of FinFET

The dynamic performance of FinFETs was investigated on 50 nm-long RF n-doped devices with 2 gate fingers of 5, 15, 25 and 30 μm-width. The fin width and the fin spacing were set to 55 and 100 nm, respectively. It is expected that these devices operate in fully depleted regime for such fin width, which was further confirmed by DC measurements. The S-parameters of the RF devices were measured in saturation ($V_d = 1.2$ V and $V_g = V_g(G_{m\max})$) up to 110 GHz

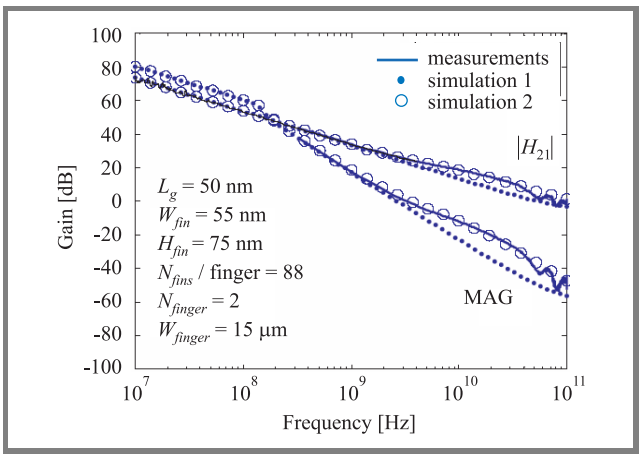

Fig. 9. Measured and simulated $|H_{21}|$ and maximum available gain (MAG) for a RF FinFET. The models considered were a classical equivalent circuit for FET (simulation 1, dots) and that of Fig. 10 (simulation 2, circles).

and the pad parasitics were removed from the raw data with an open subtraction method. In Fig. 9, the measured and modeled current gains are presented. The curve denoted as "simulation 1" was obtained with a classical equivalent circuit for FET (including a simple RC network to model the transistor input impedance) and "simulation 2" for the model shown in Fig. 10 in which a distributed

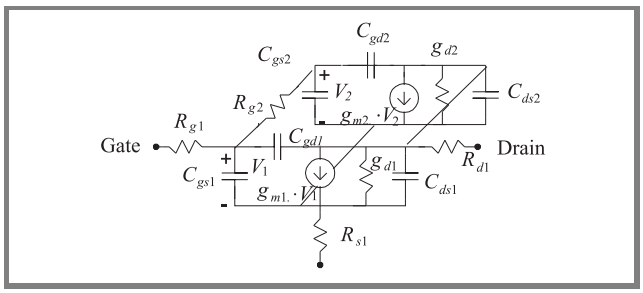

Fig. 10. Small signal equivalent circuit used for modeling the RF FinFET devices.

parasitic network (R_{g1}, C_{gs1}, C_{gd1} and R_{g2}, C_{gs2}, C_{gd2}) at the transistor input is considered. It can be seen in Fig. 9 that this improved model (circles) can closely reproduce the frequency behavior of the FinFET gain curves over the whole frequency band. The physical origin of this distributed RC at the input of the FinFET is related to the non-optimized gate silicidation (high gate resistance) and higher gate capacitance due to polysilicon residues along the silicon fins [13]. These lines of residual polysilicon are due to an incomplete polysilicon etch in the buried oxide (BOX) recess when the polysilicon gate is patterned by resist trimming. These technological problems were solved and cutoff frequencies higher than 100 GHz have been recently measured for 60 nm FinFETs [14].

6. Backgate resistance extraction of planar double gate SOI MOSFET

In the clean room facilities of Universite catholique de Louvain (UCL) we have built and measured long-channel (20 down to 1 μm) planar double gate (DG) SOI MOSFETs. The fabrication process of these DG devices is based on the transfer of a high quality thin silicon film above a pre-etched cavity in an oxide layer [15]. As shown in Fig. 11 the G_m DC value of the DG device is indeed twice higher than that of the single gate (SG) device.

As expected by the high sheet resistance of the unsilicided top polysilicon gate, a severe drop of G_m occurs above a few GHz. However, we also observe another kink in the G_m curve of the DG transistor at around a few kHz. After the extraction of a complete equivalent circuit over this wide frequency band, it was demonstrated that this G_m drop is related to the higher resistance of the back gate. This dissymmetry between the front and back gate polysilicon resistivity can be explained by the poor diffusion of doping

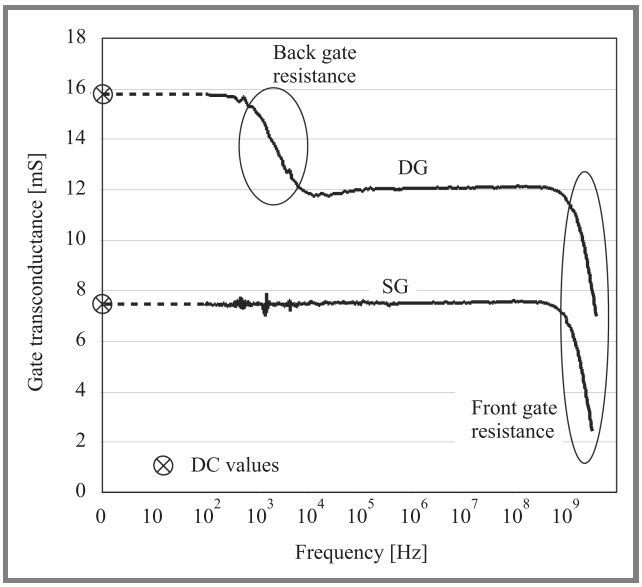

Fig. 11. Gate transconductance G_m of the measured SG and DG devices versus frequency.

atoms into the polysilicon filling the cavity. In-situ doping of the polysilicon is then required to avoid this high backgate parasitic resistance.

7. Original de-embedding technique for high input impedance MOS devices

Usually, the high frequency performance of transistors is extracted through on-wafer S-parameter measurements performed with a vector network analyzer. First, off-wafer calibration is undertaken at probe-tips using classical cali-

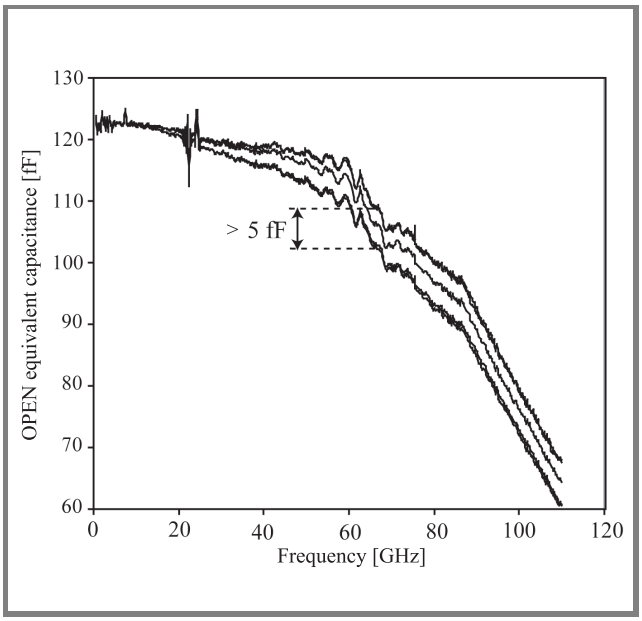

Fig. 12. OPEN capacitance versus frequency for various probing contacts.

bration techniques (LRM, LRRM, SOLT) on an alumina substrate. Then, an on-wafer de-embedding procedure is required to obtain the S-parameters of the active device. This is generally done through the use of dedicated on-wafer RF test structures (OPEN, SHORT, THRU, LINES) associated with the device under test (DUT). First of all, these RF test structures consume a non-negligible area on the wafer. Secondly, for extracting the intrinsic performance of the measured DUT, we have to probe several tests structures (i.e., OPEN, SHORT, THRU, LINES) and these multiple probings could lead to uncertainties directly related to the non-repeatability of the contact from device to device. This is illustrated in Fig. 12, which presents the equivalent capacitance of the same OPEN obtained for 5 different probing contacts. As we may observe, a variation of up to 5 fF of this capacitance can be obtained from one probing contact to another. Similar variations of the de-embedded RF structure Y-parameters were observed from one die to another on the same wafer, due to a classical spread of the technological parameters.

At the same time, MOS devices are aggressively scaled down to improve their RF performance. This contributes to a decrease of their input intrinsic capacitance, which may therefore become very small in comparison with the parasitic capacitance associated with the probing and access pads.

In order to analyze the impact of the OPEN capacitance variations on the de-embedded RF performance of advanced MOS devices, we performed some simulations using Agilent ADS. We considered a device composed of 30 gate fingers of 60 nm channel length and 500 nm gate width each, resulting in a input intrinsic capacitance of around 12 fF.

Considering a variation of the OPEN equivalent capacitance (C) from -2 fF to 2 fF, the extracted transient frequency f_T varies from 195 GHz ($C = 2$ fF) and 218 GHz ($C = 0$ fF) to 250 GHz ($C = -2$ fF). This corresponds to a variation of almost $\pm 15\%$ of the extracted f_T.

Such dispersion may be avoided when using our new de-embedding technique, in which only one probing contact is needed for performing the de-embedding of the measured DUT. This new and recently proposed [16] de-embedding technique allows us to extract the high frequency performance of a DUT without any associated RF test structure. The method is based on the behavior of the field effect transistors under ColdFET bias conditions [17, 18]. When the device is biased with V_{gs} below threshold ($V_{gs} \ll V_{th}$) and $V_{ds} = 0$ V, its intrinsic part may be neglected and the general equivalent circuit can then be simplified to the one shown in Fig. 13.

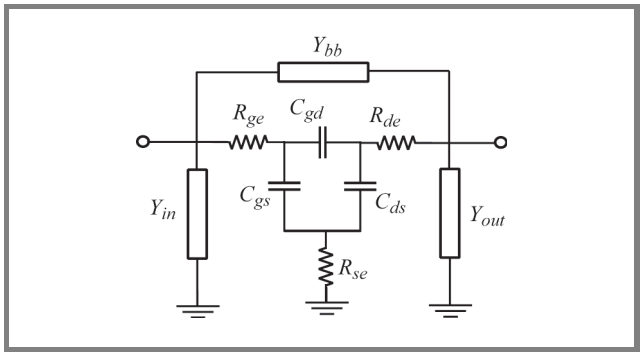

Fig. 13. Small signal equivalent circuit of the device in ColdFET bias conditions.

In addition, if we make the assumption that the transistor is symmetrical ($C_{gs} \approx C_{gd}$), the Y_{in}, Y_{out} and Y_{bb} admittances equivalent to the RF access structure, can be extracted from the measured Y_{COLD} parameters of the device in ColdFET bias conditions:

$$Y_{in} = Y_{COLD11} + 2.Y_{COLD12} + Y_{bb}\,, \tag{2}$$

$$Y_{out} = Y_{COLD22} + Y_{COLD12}\,, \tag{3}$$

$$Y_{bb} = Y_{COLD22} - Y_{COLD11} - Y_{COLD12}\,. \tag{4}$$

The RF access structure can then be de-embedded from the measured Y_{MOS} admittance matrix of the device at the bias point of interest, for instance in saturation regime ($V_{gs} > V_{th}$, $V_{ds} = V_{dd}$) with:

$$Y_{COR11} = Y_{MOS11} - Y_{in} - Y_{bb}\,, \tag{5}$$

$$Y_{COR12} = Y_{MOS12} + Y_{bb}\,, \tag{6}$$

$$Y_{COR21} = Y_{MOS21} + Y_{bb}\,, \tag{7}$$

$$Y_{COR22} = Y_{MOS22} - Y_{out} - Y_{bb}\,. \tag{8}$$

Figure 14 presents the current gain and maximum available gain obtained for a 130 nm-channel length SOI MOSFET device with 30 gate fingers of 4 and 1 μm-width, respectively. In addition, the results obtained considering a classical OPEN de-embedding procedure are plotted. A very good agreement can be observed between these two de-embedding techniques for both the current and maximum available gain.

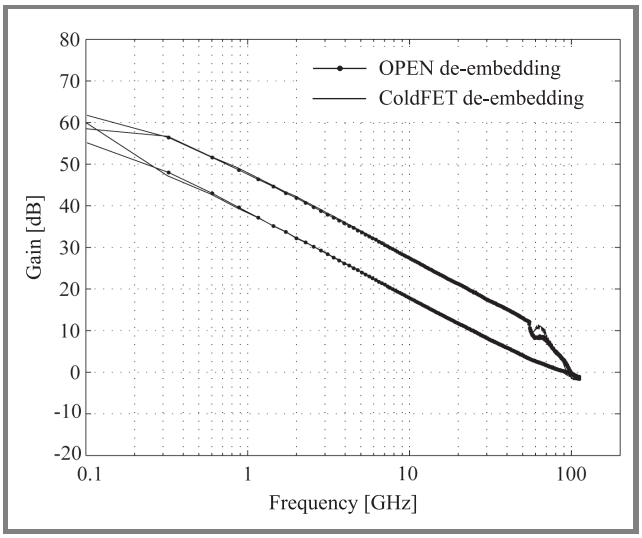

Fig. 14. Comparison of the current gain H_{21} and the maximum available gain using a classical OPEN de-embedding technique and the new ColdFET technique (NMOSFET $30 \times 4 \times 0.13$ μm^2, $V_{gs} = 0.59$ V, $V_{ds} = 1.2$ V).

To conclude, one should notice that the ColdFET de-embedding results were obtained without any other structure than the device under test and with the same probing contact for depletion and saturation regimes. This technique may save up to 50% of the wafer area (one dedicated OPEN per device is usually considered for RF test structures). Furthermore, with the downscaling process of advanced devices dimensions, the accuracy of the extracted RF performance may be affected by the dispersion and contact quality on the wafer. Our new technique allows us to break through these problems due to only one probing contact to extract the RF performance of the DUT.

8. Conclusion

From these examples, it is quite obvious that a wideband electrical characterization has to be considered at the early stage of technology development. The direct extraction of physical parameters such as parasitic capacitances, resistances, relaxation of carriers, body contact, etc., that cannot be extracted under static bias conditions is of great importance in the improvement cycle of any advanced technology. The results presented here also indicate that as transistors dimensions are continuously shrinking, it is also crucial to develop new measurement and characterization techniques in order to maintain high accuracy of the extracted parameters of advanced devices.

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