Paper

Electron mobility and drain current in strained-Si MOSFET

Jakub Walczak and Bogdan Majkusiak

Abstract— Electron mobility and drain current in a strained-Si MOSFET have been calculated and compared with the mobility and drain current obtained for the relaxed material. In the first step, our mobility model has been calibrated to the "universal mobility" according to the available experimental data for unstrained Si MOSFETS. Then, employing the mobility parameters derived in the calibration process, electron mobility and the drain current have been calculated for strained-Si MOSFETs.

Keywords— electron mobility, strained-Si MOSFET.

1. Introduction

Employing strained Si in MOSFET channel may significantly improve the performance of the device by an increase of electron mobility due to strain-induced alteration of the energy band structure. Therefore, the strained-Si technology is a promising solution for ultra-scaled devices and undergoes an intensive research work along with successful introduction to the market [1].

In this work, electron mobility and drain current for both: a relaxed-Si and a strained-Si MOSFETs have been modeled. In the first step, our mobility model has been calibrated to the "universal mobility" according to available experimental data for unstrained Si MOSFETs [2]. Then, employing the calibrated mobility model with parameters derived in the calibration process, electron mobility for a strained-Si MOSFET has been calculated, and finally, the drain current has been calculated for a strained-Si MOSFET designed as a template device for the SINANO Project Deliverable D4.14 on strained silicon [3].

2. Mobility calculation

According to the idea of this work, our electron mobility model should be calibrated to the "universal mobility" of experimental data for unstrained Si MOSFETs, and then it should be employed to a strained-Si MOSFET, with literally the same mobility parameters as those used to calculate the mobility for the unstrained device. The modeled strained devices should be bulk NMOSFETs with strained-Si channel layer resting on the $Si_{0.8}Ge_{0.2}$ virtual substrate.

Our electron mobility model is based on the relaxation time approximation, including the mobility components limited by the phonon scattering, the Coulomb scattering, and the surface roughness scattering. The effective mobility is calculated by combining these components according to Matthiessen's rule.

First, the potential and carrier concentration distributions have been obtained by self-consistent solution of 1-dimensional Poisson and Schrödinger equations, giving also quantized energy levels and envelope wave functions in the direction z perpendicular to the surface. Figure 1 shows an example of band diagram for a strained-Si bulk MOSFET, illustrating also the distribution of electron concentration, and energy levels along with the eigenfunctions (only the non-primed series of eigenstates is shown). In the calculations open boundaries have been assumed, i.e., the wave functions are allowed to penetrate into the oxide. Band offsets for strained-Si/SiGe interface are calculated according to [4, 5].

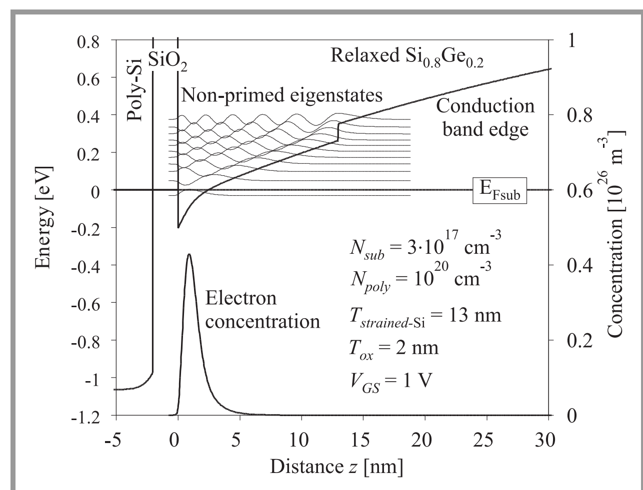

Fig. 1. Energy band diagram for a strained-Si bulk MOSFET.

A silicon layer, when grown on a $Si_{1-x}Ge_x$ substrate, is subjected to biaxial tensile strain, due to a mismatch between lattice constants of the materials under consideration. This strain rearranges the energy band structure within the strained layer. It separates the non-primed series of eigenstates from the primed series, shifting the latter up, thus promoting electron occupation in the non-primed energy subbands, which, in turn, is beneficial for electron mobility, since the transport effective mass for electrons in the non-primed subbands is smaller than for those in the primed subbands. Moreover, due to the separation of the non-primed and primed subbands, the intervalley scattering is significantly suppressed in the strained silicon. Additionally, the strain produces a discontinuity of the conduction band edge at the interface between the SiGe layer and the strained-Si layer, which can be observed in Fig. 1 as a potential step, thus confining the electrons still more within the strained channel layer. The above effects contribute to a significant mobility enhancement and make the strained silicon so attractive as a material for MOSFET channel.

Phonon scattering rates have been calculated within the approximation of isotropic effective acoustic deformation potential, which was assumed to be $D_{ac} = 12$ eV. Moreover, intervalley phonon scattering was included, and a set of phonon parameters was employed which involves a stronger coupling for intervalley phonons [6, 7] than typically used for unstrained silicon [8], and therefore reflects the mobility enhancement observed in strained-Si channels. So, the following intervalley phonons have been included: a single phonon of type-f: $E_k = 59$ meV, $D_k = 8.0 \cdot 10^8$ eV/cm, and a single phonon of type-g: $E_k = 63$ meV, $D_k = 8.0 \cdot 10^8$ eV/cm. No surface optical phonons were considered.

The matrix element for surface roughness scattering includes:

– the component due to the geometrical shift of the potential energy:

$$M_{ij} = \int \xi_i(z)\Delta_{sr} \cdot \mathrm{d}V/\mathrm{d}z(z)\xi_j(z)\mathrm{d}z, \qquad (1)$$

– the components due to the influence of the deviated plane and image potential modification [9].

The screening effect has been applied according to the Thomas-Fermi approximation with the finite extension of the wave function. Exponential spectrum was assumed with $\Delta_{rms} = 0.22$ nm, $\lambda_{sr} = 1.5$ nm.

Screened Coulomb scattering potentials induced by impurities located in the substrate were found by numerical solution of Poisson's equation [10–12] across the semiconductor and the oxide (infinite oxide thickness assumed), see Eqs. (2) and (3). No interface states and remote charges have been included:

$$\phi_{Si}(q,z,z_0) = \int_0^\infty \mathrm{d}z_1 \phi_{Si}(q,z_1,z_0) \times \Big\{ -\sum_i |\xi_i(z_1)|^2 S_i \int_0^\infty \mathrm{d}z_2 |\xi_i(z_2)|^2 \frac{1}{q} \exp(-q|z-z_2|) \Big\} + \frac{2}{2\varepsilon_{Si} q} \exp(-q|z-z_0|) + A_1 \exp(-qz), \qquad (2)$$

$$\phi_{ox}(q,z,z_0) = \frac{2}{2\varepsilon_{ox} q} \exp(-q|z-z_0|) + A_2 \exp(-qz). \qquad (3)$$

Figure 2 shows the calculated electron effective mobility as a function of the effective field for unstrained MOSFETs, compared with the experimental universal mobility curve by Takagi *et al.* [2]. Simulations for all substrate doping levels were carried out employing the same scattering parameters mentioned above, calibrated to obtain the best possible fit to the experimental data.

Figure 3 shows a comparison of the dependence of the effective mobility on the effective field for strained MOSFETs and unstrained MOSFETs for doping levels of $3 \cdot 10^{17}$ cm^{-3} and $3 \cdot 10^{18}$ cm^{-3}, while Fig. 4 presents the enhancement of electron mobility obtained in the strained devices relative to the unstrained ones, as a function of the effective field. As can be seen, strain induces a mobility enhancement of the order of several dozen per cent.

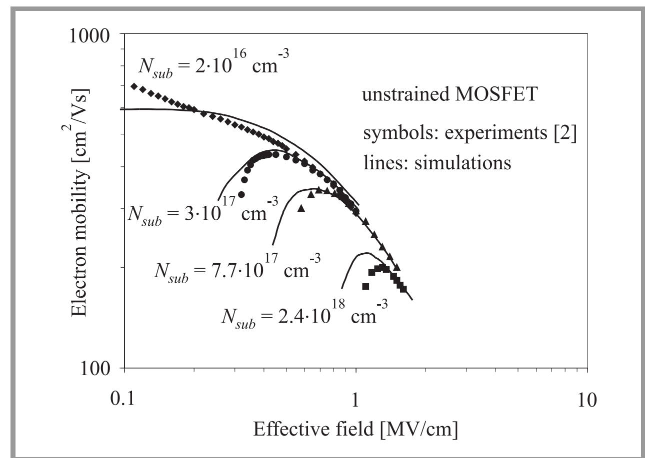

Fig. 2. Effective mobility versus effective field for unstrained MOSFETs.

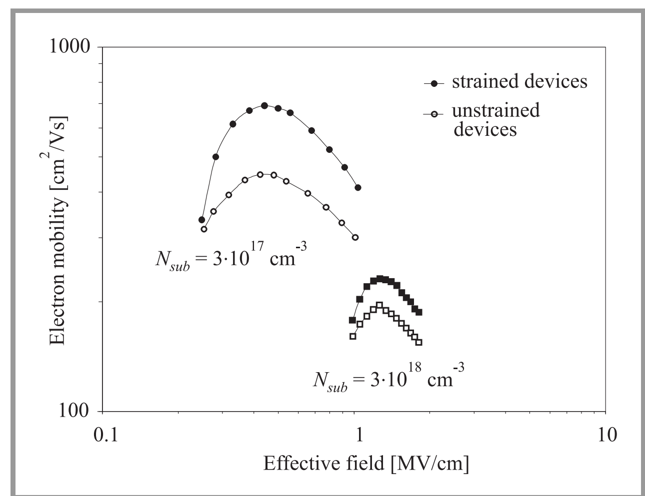

Fig. 3. Effective electron mobility versus effective field for strained and unstrained MOSFETs.

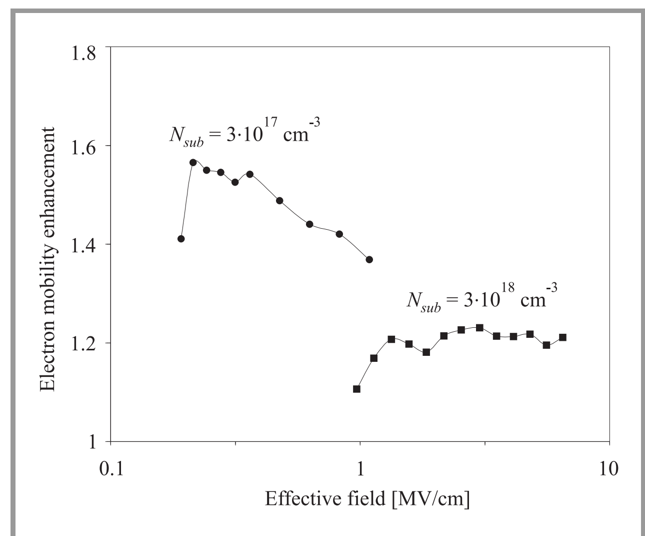

Fig. 4. Electron mobility enhancement versus effective field for two substrate doping levels.

3. Drain current calculation

Having calibrated mobility model, the next step was the calculation of the drain current for an n-channel strained-Si bulk MOSFET, which was designed as a template device for the SINANO Project Deliverable D4.14 on strained silicon. The parameters of the transistors were as follows: channel length $L = 25$ nm, oxide thickness $T_{ox} = 1.6$ nm, oxide dielectric constant $K_{ox} = 7$, acceptor doping level in the channel: $N_{sub} = 3 \cdot 10^{18}$ cm^{-3}. In spite of ultrashort channel to be modeled, we calculated the drain current within the long channel approximation, according to the Pao-Sah model [13], by integration of the product of the electron charge Q_{inv} and the electron mobility μ_{eff} over the quasi-Fermi level split u_n along the channel:

$$I_D = -\frac{W}{L}\frac{\mathrm{k}T}{q}\int_{V_{SB}}^{V_{SB}+V_{DS}} \mathrm{d}u_n\, \mu_{eff}\, Q_{inv}\,. \tag{4}$$

The current was calculated in two independent routines. First, the potential and charge distributions along with the energy levels and envelope functions were obtained and stored for all desired gate voltages and quasi-Fermi level splits related to the considered source-drain voltages. Next, the stored data were post-processed in order to calculate electron mobilities and carry out the integration according to the drain current model.

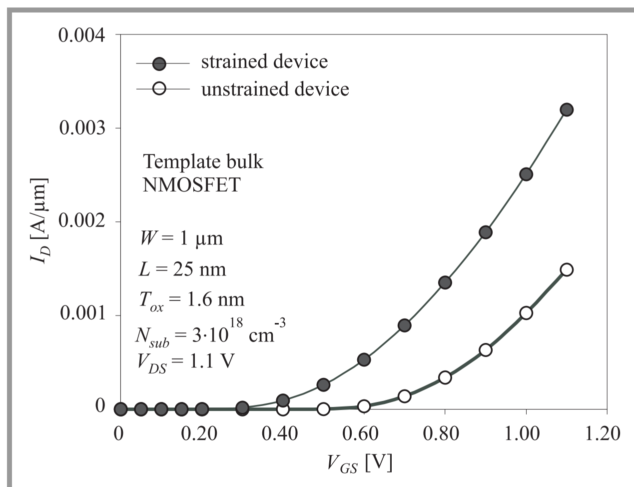

Fig. 5. Transfer characteristics for the unstrained (open symbols) and strained NMOSFETs (closed symbols).

Figure 5 shows an example of the calculated drain current transfer characteristics obtained for the drain-source voltage of 1.1 V. As a consequence of the mobility enhancement, an enhancement of the drain current is obtained for the strained-Si MOSFET.

4. Conclusions

In this work electron effective mobility and drain current for both strained-Si MOSFETs and unstrained MOSFETs have been calculated. Significant enhancements of the mobility and the current have been obtained, resulting from the biaxial tensile strain in the channel layer.

Acknowledgements

This work was supported by PULLNANO FP6 Integrated Project, contract no. 026828.

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