Paper

Optical interconnections in future VLSI systems

Grzegorz Tosik, Zbigniew Lisik, and Frederic Gaffiot

Abstract—This paper is focused on the latency and power dissipation in clock systems, which should be lower when the optical interconnects are applied. Simulation shows that the power consumed by an optical system is lower than that consumed by an electrical one, however the advantages of optics drastically decrease with the number of output nodes in H-tree. Additionally, simple replacement of an electrical system by an optical clock distribution network (CDN) results in high clock skew, which will be higher than 10% of the clock period for the 32 nm technology node.

Keywords—optical interconnects, clock skew, clock distribution network, OCDN, OVLSI.

1. Introduction

Progress of VLSI systems has been driven by the downsizing of their components and increasing operating speed. According to ITRS [1] prediction high performance integrated circuits will contain up to $2 \cdot 10^9$ transistors per chip and work with clock frequencies up to 10 GHz by 2010. One of the greatest challenges in designing such IC's is to design high-performance communication networks between their active elements. While transistor scaling provides improvements in both density and device performance, interconnect scaling improves interconnect density but generally at the cost of degraded propagation delay and power losses. In modern technologies, the interconnect delay dominates over the logic delay in spite of new metallization technologies such as copper or new low-*k* dielectrics. Signal integrity issues that occur with the global interconnect for data transfer can cause extreme problems for the clock distribution systems. Due to the bandwidth limitation of upper level interconnects the high speed clock signal cannot be distributed globally across the chip. Additionally, clock skew due to variation sources is becoming difficult to control with traditional balanced distribution networks. Since a single-chip processor available commercially consumes more than 100 W of power, thermal management is also a major concern. The main consumer (up to 30–50%) [2] of delivered power in modern IC's is the clock distribution network (CDN), that requires several hundreds of repeaters to drive the metallic tracks over the entire chip.

It becomes evident that the electrical interconnects are approaching their fundamental limits and represents the present performance bottleneck. The new materials proposed by ITRS can only extend the life of the conventional interconnect by a few years, so to meet the performance challenge, revolutionary approach will be needed. Due to such features as large bandwidth, low latency, low power requirements, reduced crosstalk, electromagnetic immunity and electrical isolation, the application of optical interconnects in VLSI systems is considered as an alternative solution.

This paper presents the estimation of the power budget and timing properties of optical clock distribution network (OCDN).

2. Optical clock distribution network

As a possible solution that can overcome problems of electrical interconnects we propose the integration of III-V active optoelectronic devices and passive silicon waveguides on the standard silicon chip as presented in Fig. 1. Silicon waveguides will be placed on the upper metallization layers and connected to the off-chip photonic source and on-chip optical receivers. To form the planar optical structure described above, the use of Si as the core and SiO_2 as the cladding materials is assumed. The Si/SiO_2 system has been chosen because it is compatible with conventional silicon technology, transparent for $1.3 - 1.55$ μm wavelength and has attenuation as low as 0.8 dB/cm [3]. Additionally, such waveguides with high relative refractive index difference $\Delta \approx (n_1^2 - n_2^2)/2n_1^2$ between the core ($n_1 \approx 3.5$ for Si) and claddings ($n_2 \approx 1.5$ for SiO_2) allow compact optical circuits to be designed and fabricated with bend radius of the order of a few micrometers. To avoid modal dispersion, improve coupling efficiency and reduce loss, single mode conditions are applied to the waveguide dimensions. The optical process is completely independent from the CMOS process and does not require a revolutionary mutation in the CMOS process.

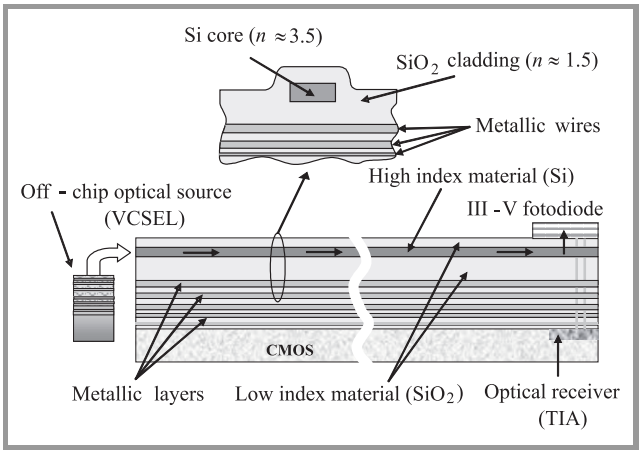

Fig. 1. Cross-section of optical interconnect structure.

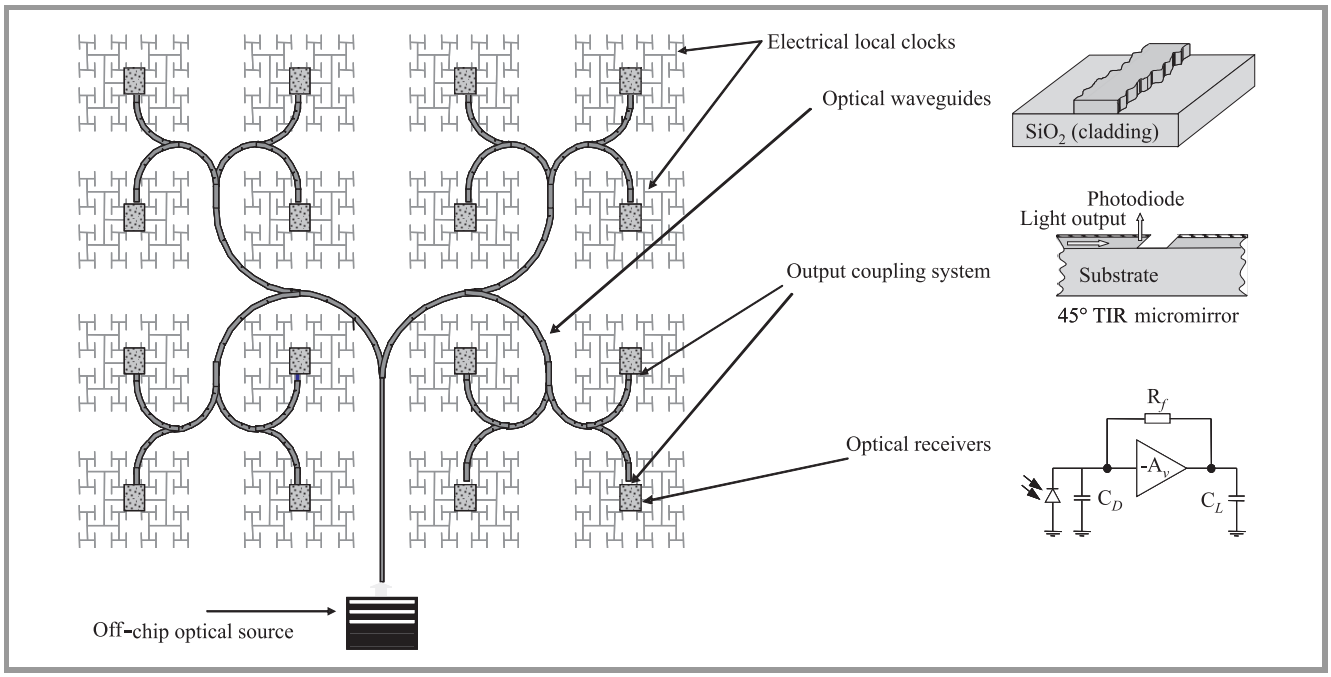

Fig. 2. General approach to optical global clock distribution network.

A tree-like structure is the most common strategy for the conventional clock system routing. This strategy is also adopted to design optical clock system. In the proposed system, shown in Fig. 2 a low-power vertical cavity surface emitting laser (VCSEL) is used as an off-chip photonic source. The VCSEL is coupled to the H-tree symmetrical passive waveguide structure and provides the clock signal to n optical receivers. The number and placement of the receivers in optical clock system is equivalent to the number and placement of the output nodes in the electrical H-tree.

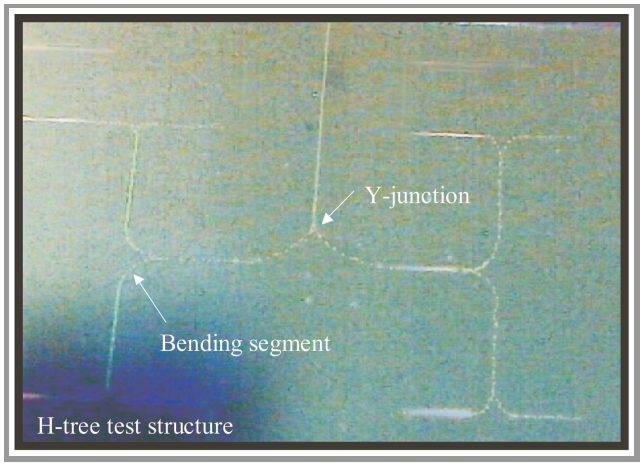

Fig. 3. Test structure of optical H-tree.

At the receivers, the high speed optical signal is converted to an electrical signal and subsequently distributed by the local electrical networks. The number of O/E converters is a particularly crucial parameter in the overall system since optoelectronic interface circuits at these points are of course necessary and consume power. The methodology and the assumptions used to properly design the optical H-tree are presented in detail in [4, 5]. Figure 3 shows a picture of the optical H-tree test structure fabricated by LETI.

3. Optical system properties

The optical alternative is, of course, acceptable only if it demonstrates significantly improved performance over the all-electrical solution. First, the power consumption of both systems is compared. The comparison is based on the ITRS technology roadmap in the case of electrical clock system and on the state-of-the-art device parameters in the case of optical clock. This assumption may result in a pessimistic estimation of the performance of the optical CDN, for future technology nodes. The results presented in Fig. 4 show the comparison between power consumption of electrical and optical clock systems both designed for the 70 nm technology node. For a small number of H-tree nodes the power

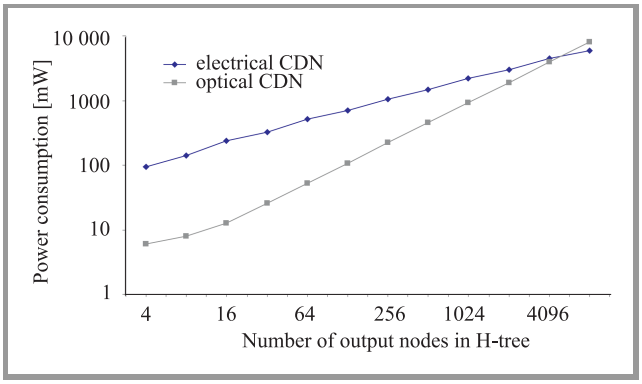

Fig. 4. Electrical power consumption of optical and electrical CDN's versus the number of H-tree nodes (20 mm chip width).

consumed by the optical H-tree is more than one order of magnitude lower than in the electrical one. However, along with the growth of circuit complexity, the advantage of the optical system tends to decrease. Finally, with 8172 output nodes in the considered case, the power consumed by the optical system becomes higher than that consumed by the electrical one. This fact can be easily explained taking into consideration the optical power budget [4, 5]. Along with doubling the number of H-tree output nodes, the optical power, which needs to be emitted by the VCSEL to meet the overall system quality increases at least by 3.2 dB (because of the Y-splitters), which in turn increases the electrical power consumed by VCSEL by more than 100%. Additionally, since the number of receivers is equal to the H-tree output nodes, the power consumed by receivers also doubles. In the case of an electrical system the power consumption increases much less rapidly. These results clearly show that the advantages of optics drastically decrease with the number of output nodes.

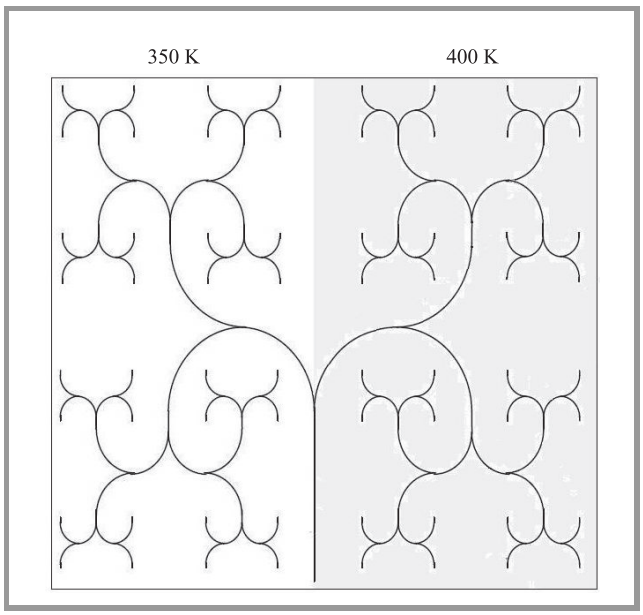

Fig. 5. Chip structure with temperature gradient.

In the next step the clock skew of the optical system is calculated. There are several sources of clock skew in optical system. Apart from process parameter variations, which are mainly the tolerance of device and waveguide physical parameters, system level fluctuations like temperature variations have to be considered. In our analysis only the impact of temperature variations on optical signal speed has been taken into account. Along with the growth of chip temperature, the refractive index of waveguide core increases thus reducing the speed of clock signal. Typical temperature gradients over the entire chip presented in literature are less then 50 K [6]. The calculation has been performed for the chip structure where the temperature of one part is lower (350 K), while that of the other part is higher (400 K) as presented in Fig. 5. This represents the worst-case scenario.

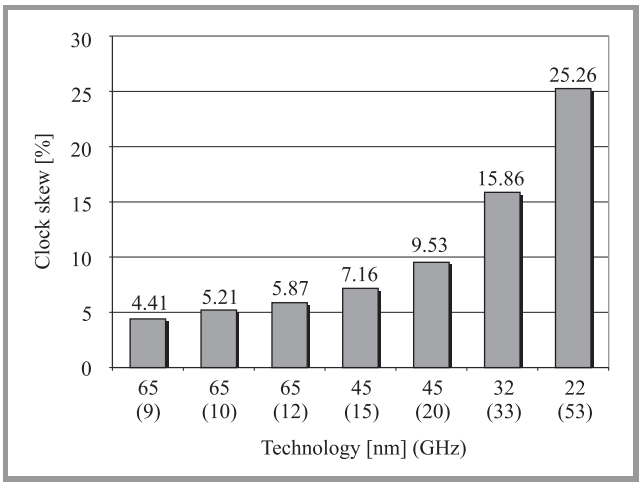

Fig. 6. Clock skew of a 64-output-node optical H-tree compared to the clock period as a function of technology.

Figure 6 shows the clock skew of a 64-output-node optical H-tree compared to the clock period as a function of technology. It is clear from this figure that just for the 32 nm technology node (33 GHz) the clock skew is higher than 10% of the clock period. This will result in a serious system failure.

4. Conclusion

Integrated optics are considered as a possible alternative to overcome metallic interconnect limitations that can be the barrier for further gigascale integration predicted by ITRS. These expectations are focused on the latency and power dissipation mainly, which should be lower when the optical interconnects are applied. In [4, 5] we demonstrate that the proposed optical solution allows the distribution of high local frequency signals across the chip with significantly lower power dissipation than the electrical one. Particularly, in the case of 45 nm technology node, the power consumed by a 256 node optical H-tree system is over 5 times less than the power dissipated in the equivalent electrical system. However, the absolute magnitude of the power dissipation in the global H-tree is a rather small part of the overall losses in the CDN system. Therefore it is necessary to increase the complexity of the optical H-tree, but the advantages of optics drastically decrease with the number of output nodes in H-tree. Additionally, a simple replacement of an electrical system by an optical CDN results in a high clock skew, which will be higher than 10% of the clock period for the 32 nm technology node. It is then clear that for the present optical technology direct replacement of classical electronic interconnections by optical ones does not exhibit a sufficient increase of the system performance (in terms of power consumption and latency). If optical interconnects are to replace metallic wires the main challenge is to develop a new generation of optoelectronics converters with low latency and low power consumption.

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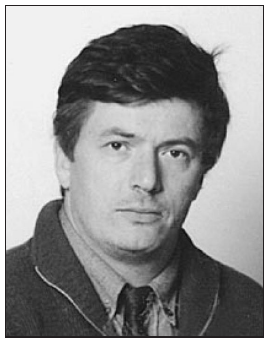
Grzegorz Tosik was born in Łask, Poland, in 1975. He received the M.Sc. degree in electronics engineering from the Technical University of Łódź (TUL), Poland, in 2000, and the Ph.D. degree in electronics from Ecole Centrale de Lyon, France, in 2004. From 2004 he is a Research and Teaching Assistant with the Institute of Elctronics at Technical University of Łódź. His research interests involve design methods modeling and simulation tools for optical SoC.
e-mail: grzegorz.tosik@p.lodz.pl
Institute of Electronics
Technical University of Łódź
Wólczańska st 211
90-924 Łódź, Poland

Zbigniew Lisik was born in Świdnica, Poland, in 1948. He received M.Sc. and Ph.D. degrees in electrical engineering from Technical University of Łódź (TUL), Poland, in 1971 and 1979, respectively. In 1992 he received D.Sc. degree in electronics from Technical University of Gdańsk. Since 2006 he is the Full Professor in electronics. Since 1980 he has been with the Institute of Electronics, TUL. He is the author of more than 200 scientific publications. His main interests are in semiconductor device modeling and manufacturing, CAD tools for power semiconductor device design, thermal management in electronics and high temperature electronics.
e-mail: zbigniew.lisik@p.lodz.pl
Institute of Electronics
Technical University of Łódź
Wólczańska st 211
90-924 Łódź, Poland



Frederic Gaffiot was born in 1959. He received the Ph.D. degree in integrated electronics from Ecole Centrale de Lyon, France, in 1987. He is currently an Associate Professor in electronics at Ecole Centrale de Lyon. He has previously worked on power devices and computer-aided design tools for analog circuits. His recent research deals primarily with the design and modeling of analog systems and microsystems.
e-mail: frederic.gaffiot@ec-lyon.fr
LEOM Ecole Centrale de Lyon
36, av. Guy de Collongue
69134 Ecully-Cedex, France