Invited paper

Gate dielectrics: process integration issues and electrical properties

Udo Schwalke

Abstract—In this work we report on the process integration of crystalline praseodymium oxide (Pr_2O_3) high-*k* gate dielectric. Key process steps that are compatible with the high-*k* material have been developed and were applied for realisation of MOS structures. For the first time Pr_2O_3 has been integrated successfully in a conventional MOS process with n^+ polysilicon gate electrode. The electrical properties of Pr_2O_3 MOS capacitors are presented and discussed.

Keywords— high-k dielectrics, CMOS, Pr_2O_3, process integration, resist removal, wet chemical cleaning, wet chemical etching, RIE.

1. Introduction

The scaling of gate dielectric thickness is a major challenge for future ULSI CMOS technologies. Only by taking advantage of in-situ gate stack processing and advanced CMOS process architectures, excellent CMOS device characteristics could be achieved with ultra-thin (1.6 nm) SiO_2 gate dielectric [1]. However, the gate oxide thickness has to be scaled down aggressively much further into the sub-1 nm regime within the next decade, according to the ITRS roadmap [2]. At such a thickness, unacceptably high direct tunneling leakage current will flow through the gate oxide. The exponential increase in tunneling current with decreasing film thickness represents a fundamental scaling limit for SiO_2. In order to overcome this barrier, the use of alternative gate dielectrics with a higher permittivity (high-*k*) is urgently needed. Due to the high-*k* values, gate dielectrics with sub-1 nm equivalent oxide thickness can be realised and show acceptable low leakage currents. Unfortunately, most of these amorphous materials are not sufficiently stable [3], change phase [4] and electrical properties at temperatures much lower than required for CMOS processing. Accordingly, the most desirable direct substitution of SiO_2 in a given CMOS process is not possible.

Very recently it was shown that crystalline praseodymium oxide (Pr_2O_3) films have excellent dielectric properties [5]. Besides an effective dielectric constant of $K_{Pr_2O_3} \approx 30$ and low leakage currents ($< 10^{-8}$ A/cm^2 @ 1 V & EOT = 1.4 nm), Pr_2O_3 films were found to be thermally stable up to 1000°C for 15 s RTA anneals in N_2 ambient. Because of these attractive properties, Pr_2O_3 appear as a suitable high-*k* replacement for SiO_2.

Although these first results are very promising, a successful CMOS process integration of crystalline high-*k* Pr_2O_3 gate dielectric requires a substantial amount of process development. Besides thermal processing, especially wet chemical etching and cleaning procedures as well as reactive ion etching (RIE), processes compatible with the new material have to be developed. In addition, process-damage effects on the high-*k* dielectric needs to be evaluated and minimised.

In this work we report on a successful attempt to integrate Pr_2O_3 directly into a given n^+ polySi gate MOS technology. The electrical properties of the MOS devices are presented and will be discussed.

2. Praseodymium oxide growth and wafer preparation

For the process integration experiments Pr_2O_3 was grown on hydrogen terminated 3″ Si(100) wafers in a multi-chamber molecular beam epitaxy (MBE) system [5]. The MBE is equipped with e-beam evaporators for Si and praseodymium oxide. Pr_2O_3 layers were grown on pre-implanted p-type Si(100) wafers at temperatures between 625 and 725°C using a commercially available ceramic Pr_6O_{11} source. The layers were subsequently covered in-situ with 50 nm undoped polySi, since unprotected Pr_2O_3 layers are not stable against air [6]. The polySi protected Pr_2O_3 wafers were transferred to the CMOS process fab of the Institut für Halbleitertechnik (IHT) at the Technische Universität Darmstadt for process development. After RCA clean and a brief HF-dip a 250 nm in-situ phosphorous doped polySi layer was deposited at approximately 750°C. The structures obtained in this way were mainly used for subsequent process development.

3. Development of key process steps

3.1. Wet chemical cleaning and etching

Wet chemical processing is extensively used in CMOS manufacturing, for cleaning, etching and resist removal. However, little is known on the compatibility of these standard procedures with high-*k* materials, especially Pr_2O_3. In order to obtain first-hand information, blanket Pr_2O_3 test samples were subjected to various wet chemical treatments. The results of wet chemical cleaning and etching

studies are summarized in Table 1. Pr_2O_3 remains stable in DI-water, HF-dip and the alkaline component of the RCA clean, and no change in the film thickness was observed by means of ellipsometry. However, Pr_2O_3 was found to dissolve in the standard RCA clean and appears unstable

Table 1
Wet chemical cleaning and etching

Procedure	Effect on Pr_2O_3
HF-dip	Appears stable
Buffered HF	Unstable
RCA clean	Soluble
RCA clean, alkaline component only	Stable
H_3PO_4	Soluble
HCl	Soluble
DI-water	Stable

in buffered HF solution. HCl solution of 0.75% was found to etch Pr_2O_3 with a high etch rate of 28 nm/min. Obviously, acid containing solutions, in particular HCl, are suitable to remove Pr_2O_3 films selectively from the silicon surface.

3.2. Resist removal

Resists used for lithography have to be removed after etching or ion implantation. However, several wet chemical methods for resist removal contain acids and are, therefore, expected to dissolve Pr_2O_3. In fact, such a behavior was observed as summarized in Table 2. Only organic solvents, like acetone or AZ100 remover, are suitable for resist stripping when Pr_2O_3 films are present.

Table 2
Resist removal

Procedure	Effect on Pr_2O_3
Acetone	Stable
H_2SO_4/H_2O_2	Soluble
HNO_3 (100%)	Soluble
AZ100 wet remover	Stable
O_2-plasma ashing	Change in film properties

Besides wet chemical treatments, resist ashing in O_2 plasma is a commonly used procedure. A clear change in film properties was observed after O_2 plasma treatment, especially the etch rate in buffered HF was found to increase compared to Pr_2O_3 reference samples. Most likely oxygen radicals produced in the plasma are incorporated in the praseodymium oxide film and/or may diffuse through and react with the Si-interface. In order to obtain further information we deposited aluminum dots on these samples and performed *CV* measurements. We observed a reduction in the dielectric constant and an increase in the threshold voltage. Both results suggest that an interfacial oxide is formed as a result of the O_2 plasma treatment, similar to the film degradation of unprotected Pr_2O_3 when exposed to air for sufficiently long times [6].

3.3. Anisotropic reactive ion etching

The development of a highly selective RIE process is another major issue for a successful process integration of praseodymium oxide in the polySi gate CMOS process.
In order to avoid damaging of the silicon substrate, the polySi gate etch has to stop at the dielectric. We found that our standard SF_6/Cl_2 process fulfills these requirements. The selectivity of the polySi-RIE against Pr_2O_3 is higher than 300 so that the process window is sufficiently large to allow for the necessary over-etching.

4. Results and discussion

4.1. Process integration of Pr_2O_3

After the appropriate RCA clean and a brief HF-dip a 250 nm in-situ phosphorus doped polySi layer was deposited on the 50 nm polySi-covered Pr_2O_3 wafers at approximately 750°C. Subsequently, the standard lithography was applied using the gate mask. The n^+ polySi gate stack is defined by anisotropic reactive ion etch using SF_6/Cl_2.

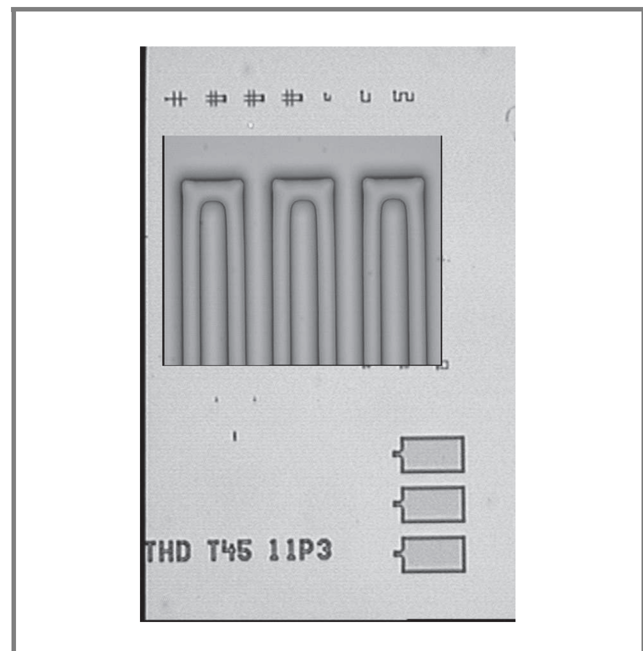


Fig. 1. Microscope image of n^+ polySi/Pr_2O_3 gate test structures after RIE. The inset shows an enlarged part of a meander structure.

In Fig. 1 a part of the test chip at the gate level is shown after the polySi gate etch. The inset in Fig. 1 shows an enlargement of a polySi meander, which is well defined. No polySi residues or damage to the Pr_2O_3 dielectric in the open areas has been observed. Also, within the uncertainty of the thickness measurements no thinning of

the praseodymium oxide was detected, confirming the high selectivity of the RIE process.

4.2. HF-CV characteristics

After wet resist strip and cleaning, the gate stack was briefly annealed at 900°C, 10 s in N_2 using RTA in order to activate the gate doping. Subsequently, electrical measurements on n^+ polySi/Pr_2O_3/Si capacitors were performed. In Fig. 2 an example of the HF-*CV* characteristic is shown.

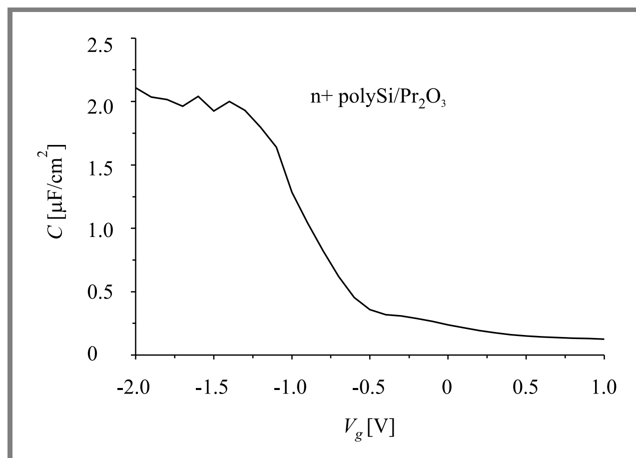


Fig. 2. HF-*CV* curve measured at 10 kHz to minimise serial resistance effects.

No evidence for hysteresis effects was noted when changing polarity of the sweep voltage within this bias range. From the accumulation capacitance of the HF-*CV* curves the effective dielectric constant was calculated $K_{Pr_2O_3} = 36$, using the physical film thickness values measured by ellipsometry. The corresponding equivalent oxide thickness EOT = $d_{Film} * (K_{SiO_2}/K_{Pr_2O_3})$ was determined as EOT = 1.8 nm, in this case without QM corrections.

4.3. Leakage characteristics

In Fig. 3 an example of the current-voltage characteristics is shown. For gate voltages below $|-3|$ V, which correspond to an equivalent field strength of approximately 22 MV/cm, the measured leakage currents are around 10 pA, which is given by the detection limit of the measurement system. The upper limit of the current density in this bias range is estimated to be $\approx 10^{-6}$ A/cm^2, in good agreement with previous results on simple gold-dot capacitors [5]. For further increased gate bias, a tunneling current starts to appear. Directly after the first sweep, a second sweep was performed. As evident from the shift in the *I-V* characteristics, significant charge trapping has occurred. The dielectric breakdown takes place at a gate bias of $|-7.5|$ V, which corresponds to a breakdown field of approximately 41 MV/cm, also in agreement with previous observations of gold-dot capacitors. However, in contrast

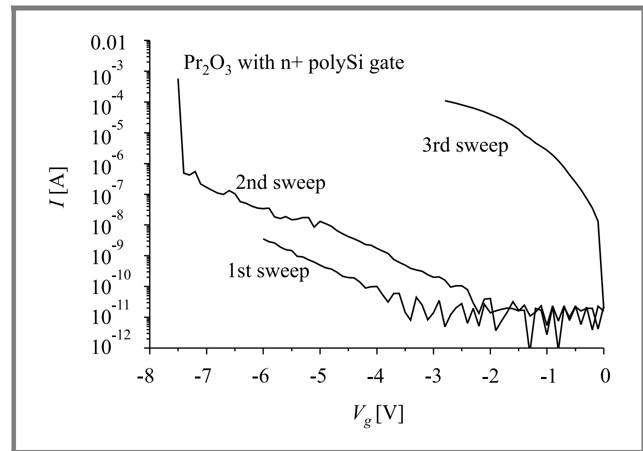


Fig. 3. Example of the current-voltage characteristics of the n^+ polySi/Pr_2O_3 MOS capacitors.

to previous findings, the breakdown was found irreversible, as evident from the 3rd sweep shown in Fig. 3.

4.4. Interface trap density and oxide charge

Admittance measurements were performed to obtain the equivalent parallel conductance G that can be used to get information on the interface trap density D_{it}. For the virgin MOS capacitor a value of $D_{it} = 3.5 \cdot 10^{11}$ /cm^2 eV is deduced from the peak conductance shown in Fig. 4. Compared to high quality device-grade SiO_2 gate oxides, this value corresponds to an increase of at least 2 orders of magnitude and is expected to degrade MOSFET device characteristics. Clearly, a substantial amount of interface engineering and optimization is needed in order to achieve the same quality level as for SiO_2.

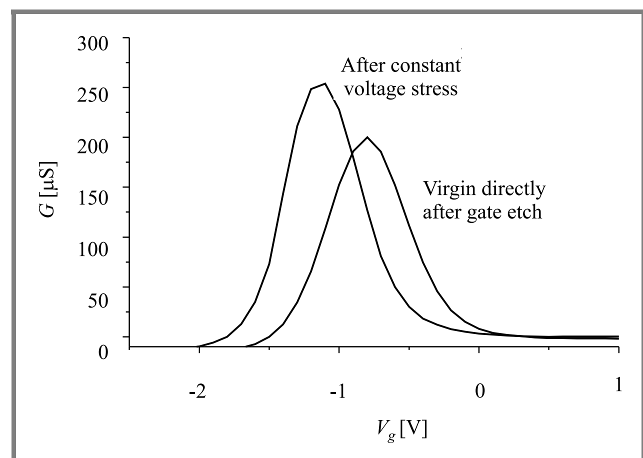


Fig. 4. Results of conductance measurements performed on virgin and electrically stressed devices.

When the Pr_2O_3 capacitor was stressed with 35 MV/cm for 10 s, an increase in interface trap density to $D_{it} = 6 \cdot 10^{11}$ /cm^2 eV was observed (Fig. 4). In addition, the peak position is shifted to further negative values, indicating

the build-up of positive trapped charge on the order of $4 \cdot 10^{12}$ q/cm^2. In this respect, the Pr_2O_3 dielectric behaves similarly to SiO_2, although the detailed mechanisms are probably quite different and require further investigation.

5. Conclusion

The crystalline high-k Pr_2O_3 material was found to be compatible with n^+ polySi gate CMOS processing when appropriate etching and cleaning procedures are used and thermal processing is restricted to RTA. We therefore conclude that a complete re-engineering of the CMOS manufacturing process may not be necessary in this case. However, the electrical characteristics of the Pr_2O_3 MOS structures reveal very high values of the interface trap density. Clearly, a substantial amount of interface engineering and optimization is needed in order to achieve the same quality level of state-of-the-art device-grade SiO_2. This is especially important in view of the fact that an enormous knowledge exists about the SiO_2/Si system used and continuously optimised in semiconductor manufacturing for more than 30 years.

References

[1] U. Schwalke, A. Gschwandtner, G. Innertsberger, and M. Keber, "Through-the-gate-implanted ultrathin gate oxide MOSFETs with corner parasitics-free shallow-trench-isolation", *IEEE EDL*, vol. 20, no. 7, 1999, p. 363.

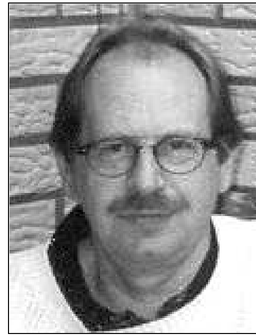
[2] The International Technology Roadmap for Semiconductor, Semiconductor Industry Association, 1999, http://public.itrs.net/Files/2003ITRS/Home2003.htm

[3] A. Kerber, E. Cartier, R. Degraeve, L. Pantisano, Ph. Roussel, and G. Groeseneken, "Strong correlation between dielectric reliability and charge trapping in SiO_2/Al_2O_3 gate stacks with TiN electrodes", in *VLSI Symp. Technol.*, Honolulu, USA, 2002.

[4] P. J. Chen, E. Cartier, R. J. Carter, T. Kauerauf , C. Zhao, J. Petry, V. Cosnier, Z. Xu, A. Kerber, W. Tsai, E. Young, S. Kubicek, M. Caymax, W. Vandervorst, S. De Gendt, M. Heyns, M. Copel, P. Bajolet, and J. Maes, "Thermal stability and scalability of Zr-aluminate-based high-k gate stacks", in *VLSI Symp. Technol.*, Honolulu, USA, 2002.

[5] H. J. Osten, J. P. Liu, P. Gaworzewski, E. Bugiel, and P. Zaumseil, "High-k gate dielectrics with ultra-low leakage current based on praseodymium oxide", *Tech. Dig. IEDM*, 2000, pp. 653–656.

[6] H. J. Osten, E. Bugiel, J. Dąbrowski, A. Fissel, T. Guminskaya, J. P. Liu, H. J. Müssig, and P. Zaumseil, "Epitaxial praseodymium oxide: a new high-k dielectric", in *Proc. Int. Worksh. Gate Insulat.*, Tokyo, Japan, 2001, pp. 100–103.



Udo Schwalke was awarded a Research Fellowship from the Alexander-von-Humboldt-Foundation for his Ph.D. thesis in 1984. During 1984–1986, he was appointed Caltech Research Fellow at the California Institute of Technology, USA. In 1987, he joined the Siemens AG, R&D Microelectronics in Munich, Germany. From 1990–1992 he was responsible for the 64 Mb DRAM device design at IBM/Siemens, USA. Subsequently, at Infineon Technologies AG (the former Siemens Semiconductor Group) he worked on novel process architectures and device reliability issues. Since August 2001, Dr. Schwalke is Professor in electrical engineering and the Managing Director of the Institute of Semiconductor Technology at the Technical University of Darmstadt. He has authored and co-authored more than 60 papers, holds several patents and is a member of IEEE and ECS.

e-mail: schwalke@iht.tu-darmstadt.de
Institut für Halbleitertechnik (IHT)
Technische Universität Darmstadt
Schlossgartenstr. 8
64289 Darmstadt, Germany