Invited paper

Silicon microelectronics: where we have come from and where we are heading

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Abstract — The paper briefly presents the history of microelectronics and the limitations of its further progress, as well as possible solutions. The discussion includes the consequences of the reduction of gate-stack capacitance and difficulties associated with supply-voltage scaling, minimization of parasitic resistance, increased channel doping and small size. Novel device architectures (e.g. SON, double-gate transistor) and the advantages of silicon-germanium are considered, too.

Keywords — MOSFET, scaling, SiGe, SOI.

1. Introduction

The silicon semiconductor industry has been a strategic part of the worldwide economy for quite some time. In the past 25 years integration, expressed as the number of transistors in an LSI (VLSI, ULSI) chip, increased approximately by a factor of 10^4 and the computational capability of an LSI chip, understood as the MIPS value of a microprocessor, increased by a factor of about 10^3. This process has had a significant impact on system performance (speed of operation and power consumption) and manufacturing costs. On the other hand, it opened new markets, where performance is of crucial importance (portable equipment, automotive industry, communications, etc.). It is being anticipated that the continuous progress in microelectronics will bring about wide-ranging social and cultural changes in the future.

The paper presents briefly the history of microelectronics development and then proceeds to discuss its limitations and possible solutions.

2. History

It can be reasonably argued that solid-state electronics began in 1945, when Bell labs established a group, lead by William Shockley, whose task was to develop a semiconductor equivalent of a vacuum tube. In 1947 John Bardeen and Walter Brattain created an amplifying circuit based on a "transfer resistance" device with point contacts. The name of the device evolved finally into a transistor. A year later William Shockley presented a revolutionary concept of a junction transistor, which had several advantages over its point-contact predecessor. In 1952 a junction field-effect transistor appeared. In 1958 Jack Kilby from Texas Instruments built a simple oscillator circuit with five integrated components. In 1959 Robert Noyce of Fairchild created a crude predecessor of today's integrated circuits using planar technology for the first time. Then, in 1960 MOSFET [1] reached a practical stage, 30 years after its concept was first presented [2]. This set the stage for the rapid development of microelectronics in the years to come.

Another important achievement was Claude Shannon's theory of communication [3]. The theory included the most fundamental issues concerning sending and processing information, that is the essence of telecommunications [4]. Among many other important aspects of the theory, Shannon defined a practical measure of information, that is a bit (binary digit). This concept was closely related to using the binary system for coding the information. Shannon's work included also the improvement of the reliability of communication by means of a certain redundancy of the information being sent over a channel.

Solid-state electronics and Shannon's theory enabled the progress in the area of data processing and communication. Before the birth of a microprocessor the functions that an integrated circuit could perform had to be implemented in the hardware, that is silicon. A microprocessor, on the other hand, could take and execute instructions that defined the function it was performing in a given application. This approach efficiently cut costs and increased enormously the versatility of the chip. The first microprocessor, 4004, was released in 1971, by Intel. The chip counted 2300 transistors and the die size was approximately 13.5 mm^2. Microprocessor 4004 was capable of performing 60000 operations in one second. Its main disadvantage was the width of its data bus – only 4 bits, which was not enough to even code the alphabet. Thus in 1972 the 8-bit version, 8008, was introduced. The chip contained about 3500 transistors. Apart from a wider data bus it could also address much more memory and had a 3–4 times higher processing power. This trend continued ever since. The subsequent microprocessors contained ever more transistors, could address more and more memory locations, their data buses were wider and they were getting faster and faster. The tendency of increasing the functionality of microprocessors is illustrated in Fig. 1, where the number of transistors in subsequent Intel processors is given.

The curve presented in Fig. 1 is a reflection of Moore's law [5]. Originally, Moore noticed that the number of components in an IC corresponding to the minimum cost per component was doubling every year.

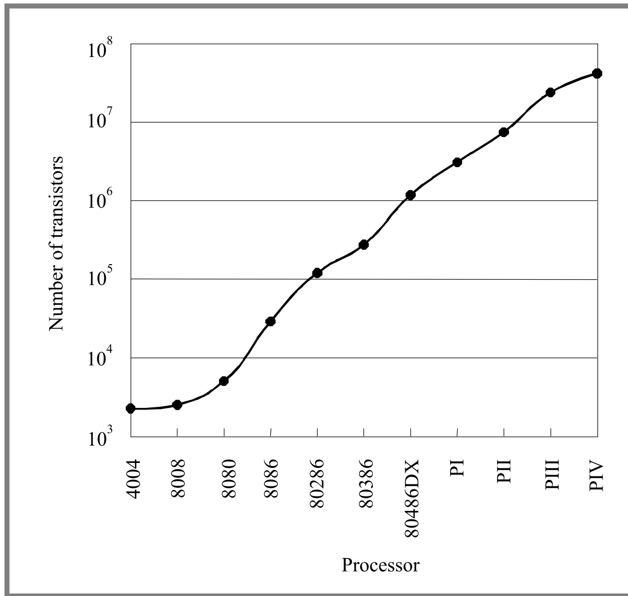

Fig. 1. Number of transistors in subsequent Intel processors (data after www.intel.com).

Later, the law had been reformulated to state that the transistor count on an IC chip doubles every 18 months. This tendency results not only from miniaturization, but also from the increase of the chip area and from improvements in the architecture, as illustrated in Fig. 2.

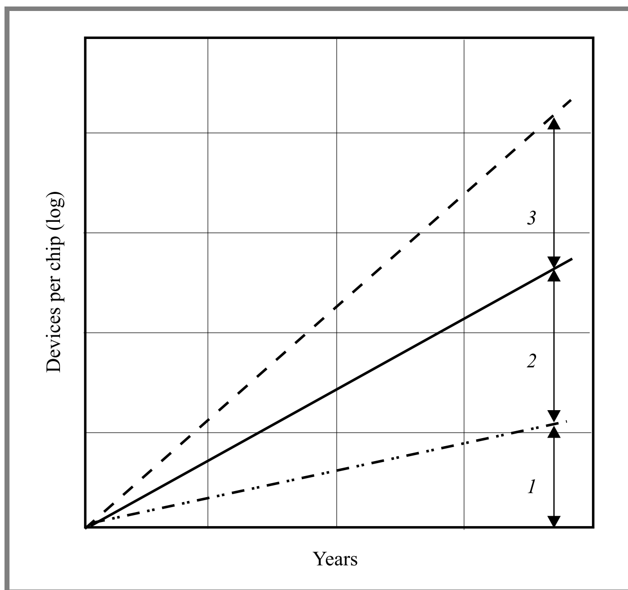

Fig. 2. Moore's law. Explanations: *1* – chip-area increase; *2* – line-width reduction; *3* – improvement of circuits and individual devices.

Moore's law has nothing to do with physics. Its persistence is rather caused by the fact that increased functionality of chips enabled by elevated transistor count causes new applications to appear. These applications, in turn, push for further progress in microelectronics. Thus a positive feedback has been created that made Moore's law a self-fulfilling prediction.

It has been argued in [6] that a shift is taking place from the world where assets were of value to the world where the value is in owning the information about assets. The boom in applications mentioned above is both the reason and the result of this shift. Moore's law is not the only one to govern the development of information technology. Robert Metcalfe, the inventor of Ethernet, predicted that the value of a network is proportional to the square of the number of nodes. This is known as Metcalfe's law [7] (Fig. 3).

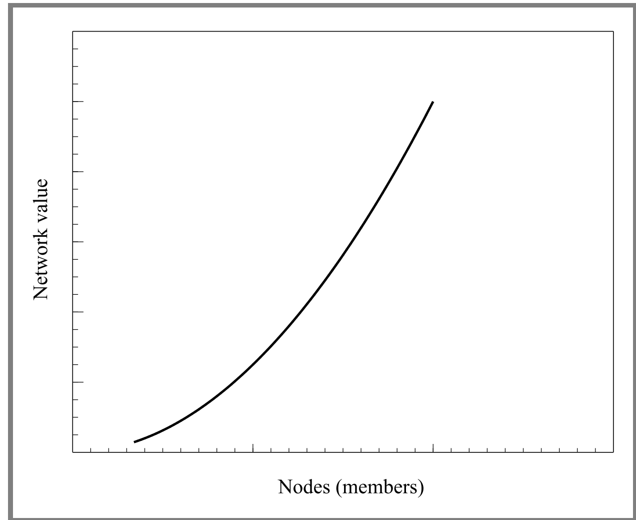

Fig. 3. Illustration of Metcalfe's law.

Another prediction, known as Gilder's law or bandwidth law, says that bandwidth grows at least three times faster than computer power [7] (Fig. 4).

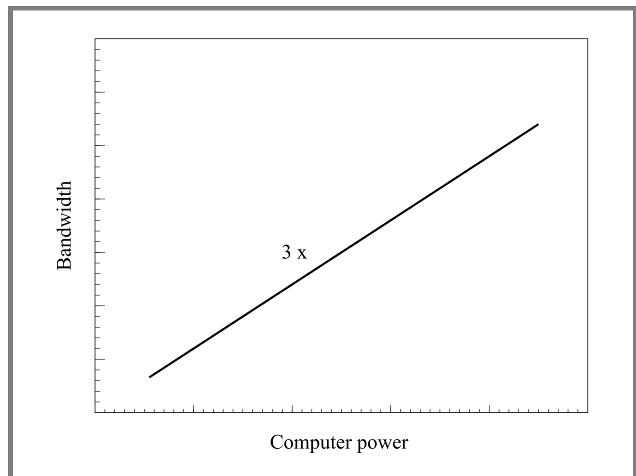

Fig. 4. Illustration of Gilder's law.

These three laws work in synergy to accelerate the development of information technology. As it was mentioned

earlier, a certain positive feedback exists between the needs created by information technology and the means to satisfy those needs, provided by microelectronics. The big question is whether the progress can be maintained forever.

3. Limits to miniaturization and possible solutions

The progress of silicon microelectronics, so far, has been driven mostly by miniaturization. The most obvious result of this process is the reduction of the dimensions of individual semiconductor devices, which, together with the improvement in the fabrication process, allows ever more devices to be crammed into one chip. The feature size F can be expressed as a function of time by the following formula:

$$F \approx \sim (7-8)\exp\left[-0.13\cdot(\text{Year}-1971)\right]\ [\mu\text{m}]. \quad (1)$$

This trend is illustrated in Fig. 5 (after [8, 9]).

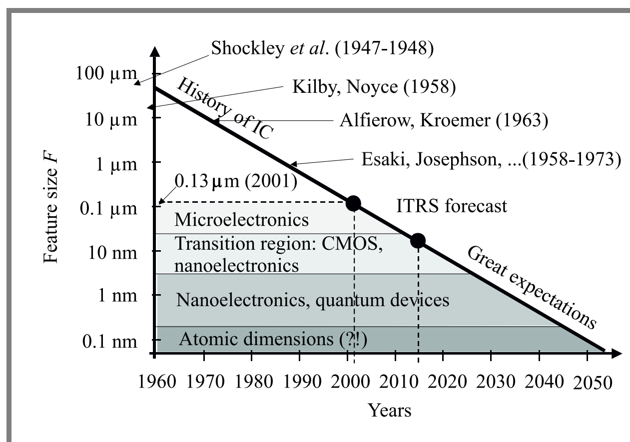

Fig. 5. Changes of feature size with time (the names and dates correspond to Nobel prizes crucial for the development of microelectronics).

The reduction of feature size, of course, increases chip functionality leading finally to a system on a chip. Reduced dimensions have yet another advantage of increased speed of operation. This is due to the shortening of the physical path the carriers have to pass and also to the reduction of the capacitances. The question is, however, how long this trend can be continued.

The main requirements for a healthy MOSFET are: high I_{ON}/I_{OFF} ratio, short-channel effects kept at a reasonable level and finite subthreshold slope. The ways to achieve this goal and the associated dangers are discussed below.

3.1. Reduction of gate-stack capacitance

The value of I_{ON} can be boosted by increasing the gate-stack capacitance. This is achieved mainly by the reduction of the gate-oxide thickness, but also by means of decreasing the gate-electrode capacitance.

Reduction of gate-oxide thickness. This step has another advantage of minimizing short-channel effects as well. The gate-oxide thickness (expressed in nanometers) has changed over the years according to the following formula (illustrated in Fig. 6):

$$t_{SiO_2} = 120\cdot\exp\left[-0.12\cdot(\text{Year}-1970)\right]. \quad (2)$$

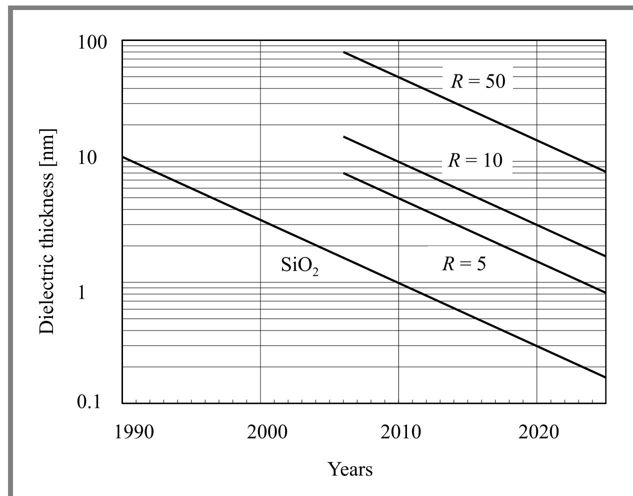

Fig. 6. Gate-oxide (SiO_2) thickness over the years. Thickness of hypothetical dielectric materials with the dielectric constant R times higher than that of SiO_2 is shown for comparison.

From the device point of view, the biggest concern associated with thin gate-oxides is the growing leakage current. Every 0.2-nm reduction between 2 and 1 nm implies a 10-fold increase of the tunneling current [10].

It has been demonstrated that even MOSFETs with the gate-oxide thickness as thin as 1.5 nm [10, 11], and even below 1 nm, can operate appropriately, on condition the channel is short. It seems, however, that increasing power consumption remains a problem, especially in terms of the entire chip rather than in terms of a single transistor. On the other hand, it is being argued [12] that with static power management the strongest limitation to the reduction of gate-oxide thickness will come from reliability, not from power-consumption concerns. While the mechanisms of thin-oxide breakdown are not understood well [13–16], it is clear that the electrical strength of a dielectric is aggravated by the roughness of the interface, especially in the case of thin layers, where a local thinning may be really dangerous. Finally, thin gate-oxides encourage the diffusion of the gate-electrode dopant into the substrate. All the above constraints indicate that there is a certain minimum gate-oxide thickness past which we cannot go.

To be sure, the operation of the final device is not the only source of the limitations of the gate-oxide thickness reduction. The formation of very thin gate-oxide layers is rather difficult [17] mainly due to extremely high reactivity of silicon surface, which cannot be maintained in the state of chemical purity for a sufficiently long time. Sufficiently

long time is understood here as that needed for loading the silicon wafers into the boat and then loading the boat into the furnace processing zone.

The other problem to be solved in the area of ultra-thin oxide formation is oxidation process controllability. In the standard, batch-type furnaces oxide growth at normally used temperatures is too fast for ultra-thin layers. As a result a compromise has to be reached between process control (and reproducibility) and oxide quality.

The answer to the problems with ultrathin SiO_2 might be the use of high-k dielectrics. Their obvious advantage is that, when compared to SiO_2, they allow for the same capacitance at much higher thickness. If the rate of gate-dielectric thinning were to be maintained, then the thickness of a hypothetical material with the dielectric constant R times higher than that of SiO_2 could be expressed with the following formula (in nanometers):

$$t_{diel} = 1.6 \cdot R \cdot \exp\left[-0.12 \cdot (\text{Year} - 2006)\right]. \quad (3)$$

Curves corresponding to the thickness of dielectric materials with $R = 5, 10, 50$ are shown in Fig. 6. Unfortunately, high-k dielectrics have to fulfill a number of requirements in order to be useful. These are [e.g. 18]: high thermal stability, perfect stoichiometry (to minimize the number of defects) low concentration of interface states and stability of the interface during thermal treatments and external radiation, resistance to dopant diffusion, sufficiently wide bandgap, sufficient barrier height for both electrons and holes. A number of high-k dielectric have been tested [e.g. 19], but it is not clear which is going to replace SiO_2 as the dominant gate-oxide material.

Reduction of gate capacitance. The other component of gate capacitance is the gate electrode made of doped polysilicon, which has the advantage of allowing for the work function adjustment by means of doping. Increased doping concentrations are also used to reduce its resistance and minimize the depletion effects. The gate capacitance degradation due to the depletion of polysilicon accounts for 0.4–0.5 nm of the equivalent oxide thickness of the total gate capacitance at inversion according to [20]. This disadvantage could be removed if polysilicon were replaced with metal. The difficulty here is, however, that the workfunction of a given metal is fixed. If a metal with midgap workfunction is used for both NMOS and PMOS, the threshold voltage will be increased by about half the bandgap [8]. To prevent this, two different metals would have to be used, with appropriate workfunctions. This would, however, complicate the fabrication process and increase costs. To make things even more ambiguous, it is being argued in [12] that poly-depletion alone, while undesirable, is not harmful enough to be the reason for replacing poly-gates with metallic ones. On the other hand, [12] proposes that poly-SiGe gate with low Ge moll fraction be used instead of poly-Si, because it allows for up to 2× reduction in poly-depletion.

3.2. Supply voltage

Another possibility of increasing the I_{ON}/I_{OFF} ratio is to increase the ratio of the supply voltage to the threshold voltage (V_{DD}/V_{TH}). Unfortunately, the V_{DD}/V_{TH} ratio is decreasing with time. It used to be around 10 for older technologies but drops to merely 4 for 0.18 μm and to less than 2 for 0.07 μm low-performance CMOS [12]. This is mostly due to the fact that oxide reliability requires appropriate reduction of the supply voltage. On the other hand, the reduction of threshold voltage is not easy because the built-in voltages inherent in the semiconductor structures are not well scalable. It is being predicted that the decrease of V_{TH} below approximately 0.25 V would result in a considerable increase of the subthreshold current [19]. Moreover, it has been demonstrated that scaling according to ITRS will lead to insufficient I_{ON} for CMOS generations of 70 nm and below [12]. Thus it is being anticipated that V_{DD} scaling will be slower than previously expected.

3.3. Minimizing the resistance

Still another way to increase I_{ON} is to minimize the parasitic series resistance, coming mainly from source and drain. The structure of a source/drain is schematically shown in Fig. 7, together with the main components of the resistance.

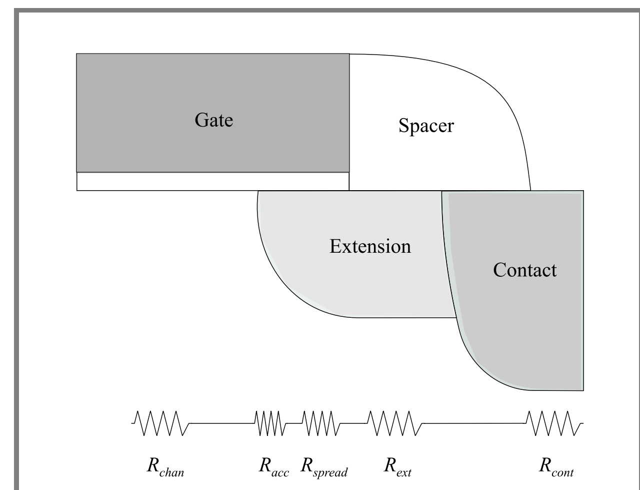

Fig. 7. Typical source/drain structure with main resistance components.

The reduction of junction depth is one of the more effective ways of controlling short-channel effects [19, 21]. This, however, increases the series resistance of a MOSFET, which can only be minimized by means of increased doping, obviously limited by maximum solid solubility. Moreover, high dopant concentrations required to minimize the resistance increase the dopant diffusivity, thus increasing the difficulties in the formation of shallow junctions resulting from thermally enhanced diffusion associated with post-implantation annealing [8]. Metastable dopant concentrations, exceeding the maximum solid solubility, could

solve the problem on condition that device processing is modified so as to minimize thermal cycles capable of dopant deactivation or that methods are found to suppress the formation of point defects facilitating deactivation [8]. A more radical solution would be to propose a different device structure.
The source and drain contacts are another source of unwanted resistance. The silicidation process, one that is used the most often to form these contacts, consumes the most highly doped portion of silicon thus further aggravating the resistance problem. This is because the resistivity of an ohmic connection between a silicide and silicon depends strongly on the doping level at the semiconductor surface. These difficulties could be potentially solved if the silicide was formed before dopant implantation or if low-temperature epitaxy could be used for silicide formation (e.g. in the case of $CoSi_2$ or $NiSi_2$) [8].

3.4. Increased channel doping

A sufficient I_{ON}/I_{OFF} ratio requires the *OFF* current to be kept at reasonable level. The control of its value can be performed by means of increased channel doping [e.g. 12]. When pushed too far, however, this may cause the source-substrate and drain-substrate junctions to act as tunneling diodes [19], with obvious consequences for device operation, not to mention mobility degradation.

3.5. Consequences of small size

The most commonly used transport models correspond to the situation where the dimensions of the devices are far greater than the mean free path. If these conditions are not fulfilled, other types of transport, usually referred to as ballistic, have to be considered [22].
On the other hand, continuous miniaturization decreases the number of atoms that an individual device consists of. The number of dopant atoms is of particular importance here, because these atoms are distributed rather randomly. Thus unintended doping non-uniformity may become a problem both in terms of a single device and in terms of unwanted differences between devices in the same integrated circuit [22].

3.6. Changing the device architecture

In view of the difficulties that seem to impede further scaling of conventional CMOS, novel device architectures have been proposed. Some of them are discussed below.

Silicon-on-insulator (SOI). A schematic cross-section of an SOI CMOS inverter is shown in Fig. 8.
The difference between conventional bulk MOSFETs and their SOI counterparts lies in the fact that the active region of a SOI MOSFET is a thin, monocrystalline silicon film separated from the rest of the substrate by a layer of buried SiO_2 or BOX. Such a design has a number of advantages. First of all due to a limited thickness of the active region the area of the source and drain junctions is much smaller, which means that the capacitance is considerably lower, therefore speed is higher. Smaller junction areas mean also that the leakage currents are lower.

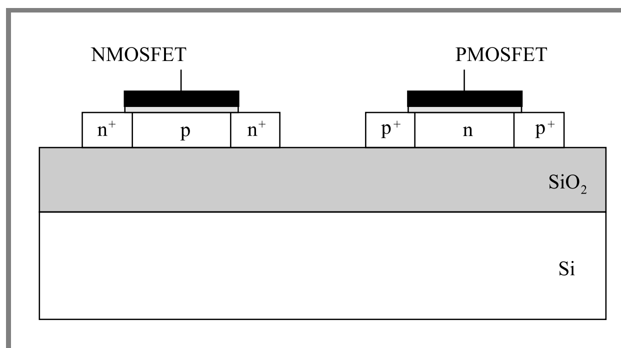

Fig. 8. A cross-section of a SOI CMOS inverter.

The SOI technology facilitates the isolation of individual devices from the rest of the circuit and thus has a considerable potential for high packaging density [23]. Another advantage is that the current driveability increases with decreasing active film, which is illustrated in Fig. 9.

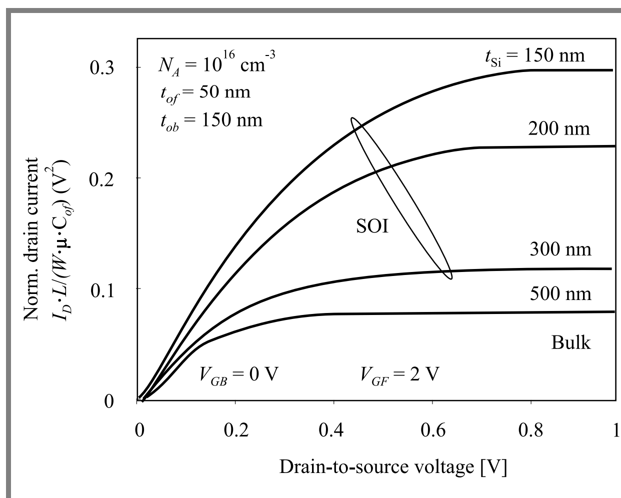

Fig. 9. Output characteristics of SOI and bulk MOSFETs [24].

While the parameters of SOI MOSFETs simulated in Fig. 8 correspond to the very beginning of SOI history, the advantages resulting from thin active region are clearly visible.
Due to the reduction of the vertical dimensions fully-depleted (FD) SOI was shown to suppress short channel effects [23]. It has been demonstrated, however, in [24] that in short-channel ($L < 0.1$ μm) FD SOI MOSFETs an electrostatic coupling between source and drain taking place via the channel and the BOX relaxes considerably the control over short-channel effects (especially the subthreshold slope).
Reducing the thickness of BOX down to 10 nm together with the reduction of the channel thickness to a similar value results in the suppression of this coupling, even for

devices with very short channels [25]. It is, however, difficult to fabricate such thin silicon and BOX layers by means of SIMOX or wafer bonding. Thus a new technology has been proposed, called silicon-on-nothing (SON). SON is aimed at fabrication of localized SOI areas under the gates of transistors within the bulk CMOS flow [26]. A schematical cross section of a SON transistor is shown in Fig. 10.

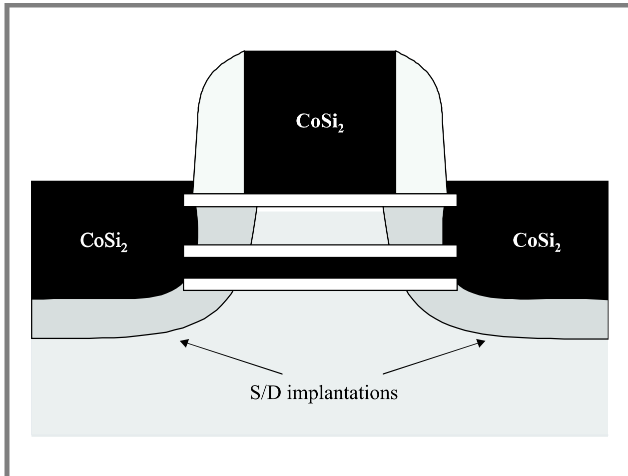

Fig. 10. A schematic cross-section of a SON MOSFET (after [25]).

This process makes it possible to form very thin layers of silicon channel and BOX (with the thickness controlled by epitaxy). Another advantage of this solution is that the buried dielectric does not reach the highly doped regions of source and drain. Therefore, the depth of the extensions is controlled by the channel thickness (which helps suppress short-channel effects), while the highly doped regions can be sufficiently deep to reduce the series resistance [25].

Double-gate MOSFET. The advantages of the double-gate transistor lie in the fact that short-channel effects are controlled by device geometry instead of doping as is the case with bulk devices. A schematic view of the double-gate transistor is shown in Fig. 11.

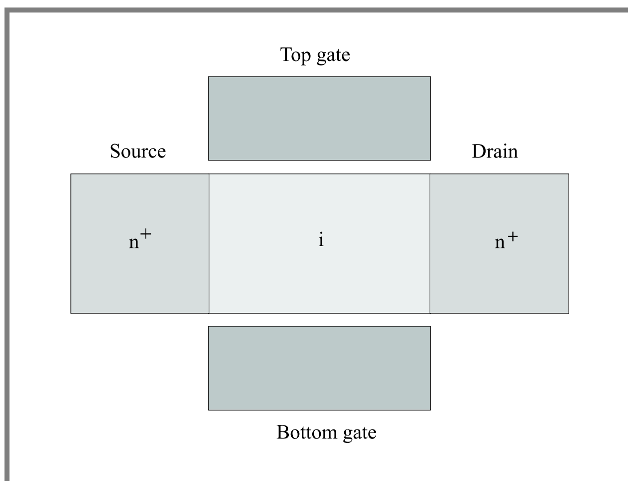

Fig. 11. A schematic view of a double-gate transistor.

The junction depth is controlled by the channel thickness. As a result, the control of short-channel effects is tighter in a DG MOSFET allowing aggressive reduction of the channel length. Thanks to the reduction of the channel doping the carrier transport is improved and the tunneling current flowing between drain and body is suppressed [20]. It is being estimated that the DG MOSFET can be scaled up to 50% further than the bulk MOSFET for some applications [27].

3.7. Silicon-germanium – increasing speed

Silicon and germanium both have the structure of a diamond. Their lattice constants are similar, there is, however, a certain lattice misfit between the two, which amounts to 4.17% at room temperature. This imposes certain constraints on the growth of SiGe layers. An important feature of SiGe is the fact that the width of its bandgap depends on the amount of germanium added (the bandgap is reduced about 7.5 mV per percent Ge). Grading Ge contents from 0 to 15% over a distance of 50–60 nm one obtains built-in electric fields of 15–20 kV/cm. Such electric fields may easily accelerate charge carriers to the saturation velocity.

This makes silicon-germanium an ideal material for the base of a bipolar transistor. The fact that the SiGe bandgap is lower than that of Si is very favourable in the case of Si emitter and SiGe base, because it enhances the injection process. Therefore the current gain of a silicon-SiGe heterojunction bipolar transistor (HBT) may be 100–1000 times higher than that of silicon BJTs (Hitachi reached $h_{FE\,\max} = 29000$). This is the case with the so-called "real" HBTs, where the germanium contents are high and constant throughout the base. Since such a high gain is not needed in practice, part of it may be sacrificed in order to allow the doping concentration in the base to be higher. This has a beneficial effect of lowering base resistance meaning higher maximum frequency of oscillations. This trade-off was impossible in conventional BJTs. Moreover, since the doping concentration of the Si base was low, the base itself could not be too thin, because of punch-through. In contrast, the thickness of a SiGe base could be scaled down, which was beneficial for the cut-off frequency. Moreover, if the germanium content is graded throughout the base from a low value at the emitter side to a high one at the collector side the transport of carriers through the base is additionally assisted by a built-in electric field, which considerably reduces transit time, leading to higher cut-off frequencies. One of the highest f_T reported so far is 350 GHz (with $f_{\max}$ of 170 GHz) and in an optimized design $f_{\max}$ of 285 GHz and f_T of 270 GHz were achieved [28]. It should be noted that in conventional BJT technology the cut-off frequency was growing at a rate of barely 4% per year. The introduction of SiGe boosted that growth to no less than 30% per year. The achieved

maximum frequencies are comparable to those obtained in HBTs based on $A_{III}B_V$ compounds and fabrication costs are significantly lower. It is being expected that SiGe will also increase the speed of operation of MOSFETs.

4. Summary

Despite increasing difficulties, the silicon technology is steadily progressing towards better functionality and higher speed of operation. Even if conventional technology reaches its limits, there will still be some room to maneuver in the form of e.g. new device architecture, especially in view of the fact that a normally operating ultra-thin channel PMOSFET with gate length of 6 nm has already been reported [29]. It should be remembered, however, that miniaturization, apart from simple reduction of size, brings about also significant qualitative changes. Some of those are illustrated in Table 1. The reduction of the number of dopants in the active region poses obvious problems for those involved in device fabrication. Those involved in device modeling will have to find a way to describe the operation of such devices. Finally, the incredible speed they offer will surely have huge impact on the design of integrated circuits, since the delay problem will increasingly shift from devices to interconnects.

Table 1
MOSFET evolution

Parameter	Past	Present	Future
Channel length	1 μm	0.1 μm	0.01 μm
Number of dopant atoms in the active region	$\sim 10^6$	$\sim 10^6$	e.g. 3
Number of electrons participating in the switching process	$\sim 10^7$	$\sim 10^4$	e.g. 30
Cut-off frequency	1 GHz	100 GHz	> 1 THz

On the other hand, it may be argued that microelectronics is slowly reaching the stage where the value moves from the technology itself to its application. In such circumstances, it is rather difficult to predict the future, and maybe the best approach towards it is that of Albert Einstein, who once said: "I never worry about the future. It comes soon enough".

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