

# Critical modeling issues of SiGe semiconductor devices

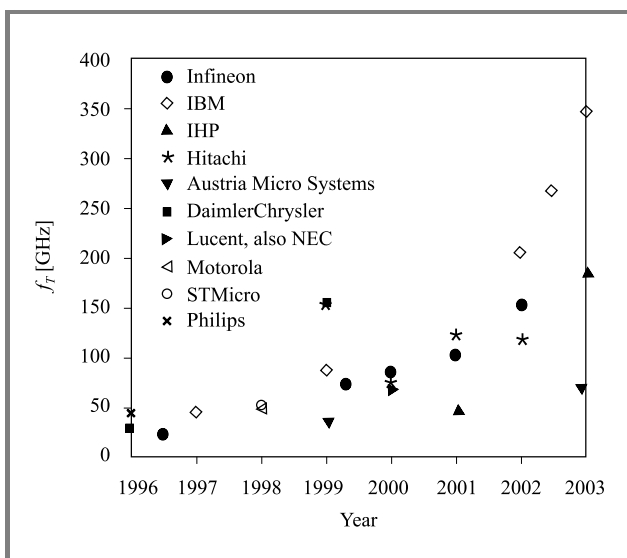
Vassil Palankovski and Siegfried Selberherr

**Abstract** — We present the state-of-the-art in simulation of silicon-germanium (SiGe) semiconductor devices. The work includes a detailed comparison of device simulators and current transport models. Among the critical modeling issues addressed in the paper, special attention is focused on the description of the anisotropic majority/minority electron mobility in strained SiGe grown on Si. We use a direct approach to obtain scattering parameters ( $S$ -parameters) and other derived figures of merit of SiGe heterojunction bipolar transistors (HBTs) by means of small-signal AC-analysis. Results from two-dimensional hydrodynamic simulations of SiGe HBTs are presented in good agreement with measured data. The examples are chosen to demonstrate technologically important issues which can be addressed and solved by device simulation.

**Keywords** — SiGe HBT, numerical simulation, modeling, bandgap, mobility, small-signal simulation,  $S$ -parameters.

## 1. Introduction

SiGe HBTs progressively replace III-V devices for their typical applications, such as low noise amplifiers and frequency dividers up to 99 GHz [1], and are considered essential for 40 Gbit/s optical communication systems. Transit frequencies,  $f_T$ , of 350 GHz [2], maximum oscillation frequencies,  $f_{max}$ , of 285 GHz, and ring oscillator delays of 4.2 ps [3] have been reported. Figure 1 shows the rapid



**Fig. 1.** Current gain cutoff frequency  $f_T$  of SiGe HBTs over time.

progress of peak- $f_T$  of SiGe HBTs over the last couple of years. The devices are fully compatible with the existing state-of-the-art 0.13  $\mu\text{m}$  CMOS technology [3, 4]. Digital application-specific integrated circuits (ASICs) are combined with SiGe HBT circuits in the so-called SiGe BiCMOS technology and are in volume production.

With the shrinking of device dimensions and replacement of hybrid mounted transistors by MMICs, rigorous physical device simulation and circuit simulation with distributed devices has to be carried out by simulation tools which account for physical effects on a microscopic level. Optimization of geometry, doping, materials, and material composition is targeting high power, high breakdown, high speed (high  $f_T$ ,  $f_{max}$ ), low leakage (low power consumption), low noise, etc. This is a challenging task that requires significant efforts in device modeling.

Section 2 gives a review of state-of-the-art device simulators and discusses the choice of current transport models to be used. In Section 3 critical modeling issues are addressed, such as bandgap narrowing, anisotropic electron minority mobility in strained SiGe, carrier transport through heterointerfaces, carrier generation/recombination, and lattice self-heating.

Section 4 presents numerical simulation results compared to the experimental data for SiGe HBTs. The examples are chosen to demonstrate technologically important issues which can be addressed and solved by device simulation. In particular, examples were chosen, where physical effects are of importance for both the DC-, and the AC- device behavior, e.g. forward characteristics of SiGe HBTs with different Ge contents considering band gap narrowing and anisotropic mobility effects, output characteristics including self-heating and impact-ionization generation effects, and  $f_T$  vs.  $I_C$  plots accounting for hot-carrier effects and anisotropic transport. All obtained results are in good agreement with the measured data.

## 2. Device simulators

The continuously increasing computational power of computer systems allows the use of technology computer aided design (TCAD) tools on a very large scale. Several commercial device simulators, e.g. [5–10], company-developed simulators, e.g. [11, 12], and university developed simulators, e.g. [13–19], claim the capability to handle SiGe devices. These simulators differ considerably in dimensionality (one-, /quasi-/two-, or /quasi-/three-dimensional), in the choice of carrier transport model (drift-diffusion, energy-

Table 1  
Comparison of device simulators

Simulator	Dimension	Model	Features
NEMO	1D		Schrödinger-Poisson solver
BIPOLE3	Quasi-2D	DD	Polysilicon
ATLAS	2D	DD, ET	TE heterojunction model
APSYS	2D	HD	Optical, interfaces
Jungemann	2D	DD, HD, MC	Rigorous transport modeling
PISCES	2D	DD, ET	Polysilicon, harmonic balance
MEDICI	2D	DD, HD	Anisotropic properties
FIELDAY	2D, 3D	DD	Electrothermal
Minimos-NT	2D, 3D	DD, HD	(See Section 3)
DESSIS	2D, 3D	DD, HD	Trap modeling, TFE model
DD – drift-diffusion, ET – energy-transport, HD – hydrodynamic			

transport, or Monte Carlo statistical solution of the Boltzmann equation), and in the capability of including electrothermal effects. The drift-diffusion transport model [20] is by now the most popular model used for device simulation. With down-scaling feature sizes, non-local effects become more pronounced and must be accounted for by applying an energy-transport or hydrodynamic transport model [21]. During the last two decades Monte Carlo methods for solving the Boltzmann transport equation have been developed [22, 23] and applied for device simulation [24–26]. However, reduction of the demand on computational resources is still an issue and, therefore, Monte Carlo device simulation is still not feasible for industrial application on a daily basis. A way to preserve the accuracy at lower computational cost is to calibrate lower order transport models to Monte Carlo simulation data.

In addition, quantum mechanical effects are often neglected or accounted for only by simple models for quantum corrections [27, 28], as solving the Schrödinger or the Wigner equation is extremely expensive in terms of computational resources.

The limited feedback from technological state-of-the-art process development to simulator development is a common drawback. The quality of the physical models can be questioned as the model parameters for SiGe are often simply inherited from parameters for silicon. Critical issues concerning simulation of heterostructures are frequently not considered, such as interface modeling at heterojunctions and at silicon/polysilicon interfaces. Hydrodynamic and high field effects, such as carrier energy relaxation, impact ionization, and self-heating effects, are often ignored.

The two-dimensional device simulator PISCES [13], developed at Stanford University, incorporates modeling capabilities for SiGe based devices, e.g. for silicon/polysilicon interfaces. One of its versions, PISCES-HB, includes harmonic balance for large signal simulation.

The device simulator MEDICI from Synopsis [10], which is also based on PISCES, offers simulation features for SiGe/Si HBTs. Advantages of this simulator are hydrodynamic simulation capabilities and a rigorous approach to generation/recombination processes. In addition, it includes

a module treating anisotropic material properties. This simulator has some weakness in the capability of mixed-mode device/circuit simulation.

At the quantum level, among others, a one-dimensional Schrödinger-Poisson solver NEMO [12], based on non-equilibrium Green's functions, is offered for sub-0.1  $\mu\text{m}$  SiGe structures.

The two- and three-dimensional device simulator DESSIS from ISE [8] has demonstrated a rigorous approach to semiconductor physics modeling. Various critical issues, such as extensive trap modeling, are solved.

Quasi-two-dimensional approaches using a simplified one-dimensional current equation are demonstrated, among others, by BIPOLE3 from BIPSIM [7] which additionally features good models for polysilicon.

The two-dimensional Fast Blaze from Silvaco [6] has capabilities of simulating heterostructure devices. Simulations of SiGe HBTs were announced, based on a simulator originally developed at the University of Ilmenau, PROSA [18]. However, in the latter no material interfaces are considered. Several good optimization results for SiGe HBTs were achieved with another university developed simulator, SCORPIO [29].

Table 1 summarizes features of SiGe device simulators discussed in this paper.

### 3. Critical issues of modeling SiGe devices

This section discusses critical modeling issues for SiGe semiconductor devices. We have addressed these issues in our three-dimensional device simulator Minimos-NT [19], which can deal with different complex structures and materials, such as SiGe and various III-V binary and ternary compounds, with arbitrary material composition profiles in a wide temperature range.

The models are based on experimental or Monte Carlo simulation data and employ analytical functional forms which cover the whole material composition range. The model parameters are checked against several independent technolo-

gies to obtain a concise set used for all simulations. Re-viewing simulation of HBTs and submicron heterojunction field-effect transistors with gate-lengths down to 100 nm, solutions of energy transport equations are necessary to account for non-local effects, such as velocity overshoot. A model for carrier temperature dependent energy relaxation times [30] has been developed as well as a model for lattice temperature dependent saturation velocities [31].

Heterointerface modeling is a key issue for devices which include abrupt junctions. Thermionic emission and field emission effects critically determine the current transport parallel and perpendicular to the heterointerfaces.

All important physical effects, such as bandgap narrowing, anisotropic electron minority mobility in strained SiGe, Shockley-Read-Hall recombination, surface and Auger recombination, and impact ionization are taken into account. III-V materials and SiGe are known to have a reduced heat conductivity in comparison to silicon [32]. Self-heating effects are accounted for by solving the lattice heat flow equation self-consistently with the energy transport equations. Examples are given in Section 4 for SiGe HBTs.

Advanced device simulation allows a precise physics-based extraction of small-signal parameters [33, 34]. Measured bias dependent  $S$ -parameters serve as a valuable source of information when compared at different bias points to simulated  $S$ -parameters from a device simulator, such as Minimos-NT. This procedure reflects the full RF-information contained in the  $S$ -parameters and allows process control beyond the comparison of DC-quantities.

### 3.1. Bandgap and bandgap narrowing

Modeling of strained SiGe is not a trivial task, since attention has to be focused on the stress-dependent change of the bandgap due to Ge content [35].

The temperature-dependent bandgaps of the constituents,  $E_g^{\text{Si}}$  and  $E_g^{\text{Ge}}$ , are calculated by the commonly used model of Varshni [36]

$$E_g = E_{g,0} - \frac{\alpha \cdot T_L^2}{\beta + T_L}, \quad (1)$$

where  $E_{g,0}$  is the bandgap at  $T_L = 0$  K. The parameter values are summarized in Table 2. The dependence on the material composition  $x$  is then introduced by

$$E_g^{\text{SiGe}} = E_g^{\text{Si}} \cdot (1-x) + E_g^{\text{Ge}} \cdot x + C_g \cdot (1-x) \cdot x \quad (2)$$

with a bowing parameter  $C_g = -0.4$  eV. This one-valley bandgap fit can be applied to the case of the technologically important strained  $\text{Si}_{1-x}\text{Ge}_x$  grown on Si (see Fig. 2).

Table 2

Parameter values for modeling the bandgap energy

Material	$E_{g,0}$ [eV]	$\alpha$ [eV/K]	$\beta$ [K]
Si	1.1695	$4.73 \cdot 10^{-4}$	636
Ge	0.7437	$4.774 \cdot 10^{-4}$	235

Depending on the strain the bandgap can become smaller than the one of pure Ge [37] in certain cases. In the unstrained case, however, an  $X$ -to- $L$  gap transition is observed at about  $x = 0.85$ , which has to be accounted by the model as well.

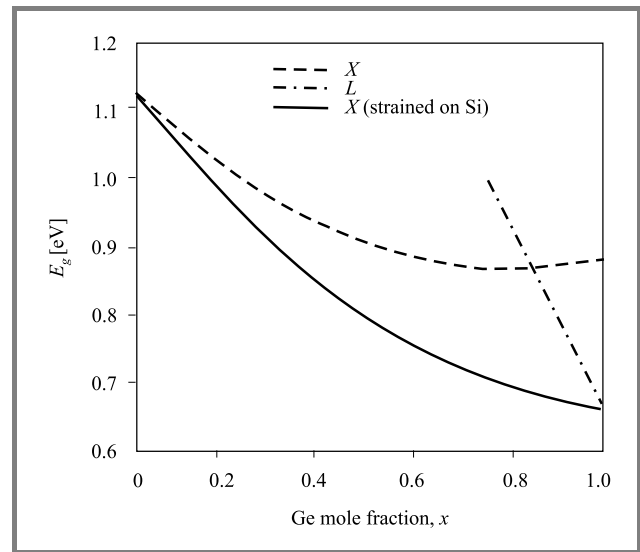


Fig. 2. Material composition dependence of the  $L$  and  $X$ -bandgaps in  $\text{Si}_{1-x}\text{Ge}_x$  at 300 K.

The stress-dependent change of the bandgap is an effect which must be separated from dopant-dependent bandgap narrowing (BGN) which for itself depends on the semiconductor material composition, the doping concentration, and the lattice temperature [38].

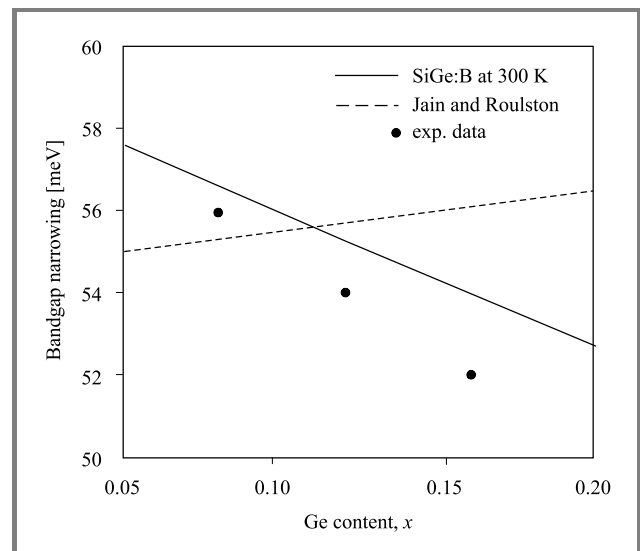


Fig. 3. Doping-dependent bandgap narrowing versus Ge content in p-SiGe compared to experimental data.

In Fig. 3 BGN versus material composition in boron-doped  $\text{Si}_{1-x}\text{Ge}_x$  is compared to another model [39]. The decrease of the BGN with increase of the Ge fraction was already experimentally observed [40, 41]. Our theoretical approach

explains this effect by the decreased density of states in the valence band and an increase of the relative permittivity in the strained SiGe alloy.

### 3.2. Carrier mobility

As the minority carrier mobility is of considerable importance for bipolar transistors, an analytical low field mobility model which distinguishes between majority and minority electron mobilities has been developed [38] using Monte Carlo simulation data for electrons in Si. A similar expression is currently implemented in Minimos-NT:

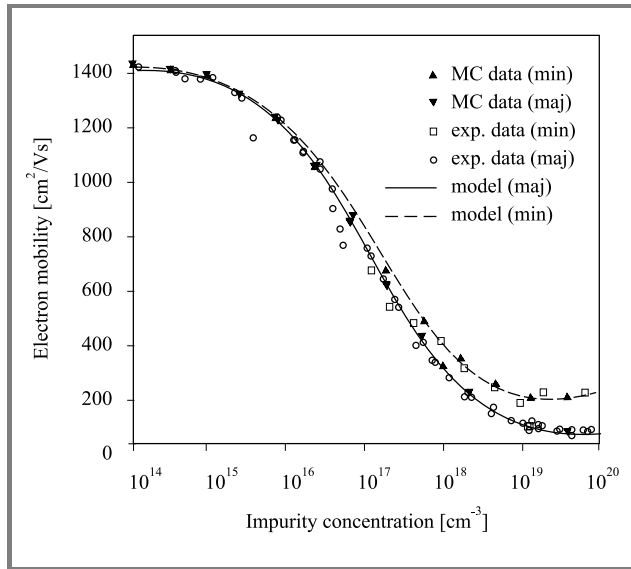
$$\mu_n^{\text{maj}} = \frac{\mu_n^L - \mu_{\text{mid}}^{\text{maj}}}{1 + \left(\frac{N_D}{C_{\text{mid}}}\right)^\alpha} + \frac{\mu_{\text{mid}}^{\text{maj}} - \mu_{\text{hi}}^{\text{maj}}}{1 + \left(\frac{N_D}{C_{\text{hi}}^{\text{maj}}}\right)^\beta} + \mu_{\text{hi}}^{\text{maj}}, \quad (3)$$

$$\mu_n^{\text{min}} = \frac{\mu_n^L - \mu_{\text{mid}}^{\text{min}}}{1 + \left(\frac{N_A}{C_{\text{mid}}}\right)^\alpha} + \frac{\mu_{\text{mid}}^{\text{min}} - \mu_{\text{hi}}^{\text{min}}}{1 + \left(\frac{N_A}{C_{\text{hi}}^{\text{min}}}\right)^\beta} + \mu_{\text{hi}}^{\text{min}}, \quad (4)$$

where  $\mu^L$  is the mobility for undoped material,  $\mu_{\text{hi}}$  is the mobility at the highest doping concentration.  $\mu_{\text{mid}}^{\text{maj}}$ ,  $\mu_{\text{hi}}^{\text{maj}}$ ,  $\mu_{\text{mid}}^{\text{min}}$ ,  $\mu_{\text{hi}}^{\text{min}}$ ,  $C_{\text{mid}}$ ,  $C_{\text{hi}}^{\text{maj}}$ ,  $C_{\text{hi}}^{\text{min}}$ ,  $\alpha$ , and  $\beta$  are used as fitting parameters. The final low-field electron mobility  $\mu_n^{\text{LI}}$ , which accounts for a combination of both acceptor and donor doping is given by

$$\mu_n^{\text{LI}} = \left( \frac{1}{\mu_n^{\text{maj}}} + \frac{1}{\mu_n^{\text{min}}} - \frac{1}{\mu_n^L} \right)^{-1}. \quad (5)$$

Figure 4 demonstrates a good match between the analytical model, our Monte Carlo simulation data, and measurements from [42–45] at 300 K for Si.



**Fig. 4.** Majority and minority electron mobility in Si at 300 K: comparison between Monte Carlo simulation data and experimental data.

Monte Carlo simulation which accounts for alloy scattering and the splitting of the anisotropic conduction band valleys

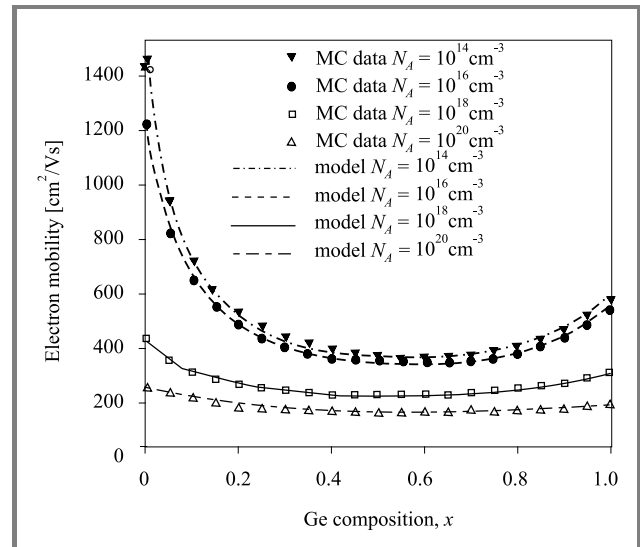
due to strain [46] in combination with an accurate ionized impurity scattering model [47] allowed us to obtain results for SiGe for the complete range of donor and acceptor concentrations and Ge contents  $x$ . We use the same functional form to fit the doping dependence of the in-plane mobility component for  $x = 0$  and  $x = 1$  (Si and strained Ge on Si). The material composition dependence is modeled by

$$\frac{1}{\mu(x)} = \frac{1-x}{\mu^{\text{Si}}} + \frac{x}{\mu^{\text{Ge}}} + \frac{(1-x) \cdot x}{C_\mu} \quad (6)$$

$C_\mu$  is a bowing parameter which equals 140 cm<sup>2</sup>/Vs and 110 cm<sup>2</sup>/Vs for doping levels below and above  $C_{\text{mid}}$ , respectively. Figure 5 shows the in-plane minority electron mobility in Si<sub>1-x</sub>Ge<sub>x</sub> as a function of  $x$  at 300 K for different acceptor doping concentrations. The model parameters used for SiGe at 300 K are summarized in Table 3.

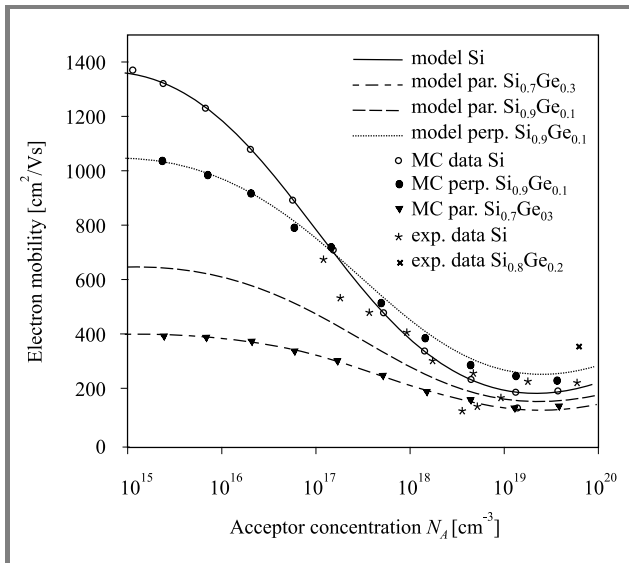
Table 3  
Parameter values for the majority/minority electron mobility at 300 K

Parameter	Si	Ge(on Si)	Unit
$\mu_n^L$	1430	560	cm <sup>2</sup> /Vs
$\mu_{\text{mid}}^{\text{maj}}$	44	80	cm <sup>2</sup> /Vs
$\mu_{\text{hi}}^{\text{maj}}$	58	59	cm <sup>2</sup> /Vs
$\mu_{\text{mid}}^{\text{min}}$	141	124	cm <sup>2</sup> /Vs
$\mu_{\text{hi}}^{\text{min}}$	218	158	cm <sup>2</sup> /Vs
$\alpha$	0.65	0.65	
$\beta$	2.0	2.0	
$C_{\text{mid}}$	$1.12 \cdot 10^{17}$	$4.0 \cdot 10^{17}$	cm <sup>-3</sup>
$C_{\text{hi}}^{\text{maj}}$	$1.18 \cdot 10^{20}$	$4.9 \cdot 10^{18}$	cm <sup>-3</sup>
$C_{\text{hi}}^{\text{min}}$	$4.35 \cdot 10^{19}$	$5.4 \cdot 10^{19}$	cm <sup>-3</sup>



**Fig. 5.** Minority electron mobility in Si<sub>1-x</sub>Ge<sub>x</sub> as a function of  $x$  for in-plane direction: the model is in good agreement with Monte Carlo simulation data.

The component of the mobility perpendicular to the surface is then obtained by a multiplication factor given by the ratio of the two mobility components. The good agreement of the model with the measured and the Monte Carlo simulation data, both for in-plane and perpendicular to the surface directions, is illustrated in Fig. 6.



**Fig. 6.** Minority electron mobility in  $\text{Si}_{1-x}\text{Ge}_x$  as a function of  $N_A$  and  $x$ : the model is in good agreement with measurements and Monte Carlo simulation data both for in-plane and perpendicular to the surface directions.

## 4. Analyzed SiGe HBT structures

In this section we analyze SiGe HBTs from an industrial vendor. The devices are part of proven  $0.8\ \mu\text{m}$  and  $0.35\ \mu\text{m}$  BiCMOS technologies which include CMOS process and high-performance analog-oriented HBT module. The applications reach from circuits for mobile communication to high-speed networks.

Our methodology for characterization and optimization of SiGe HBTs involves process calibration, device calibration employing two-dimensional device simulation, and automated technology computer aided design optimization.

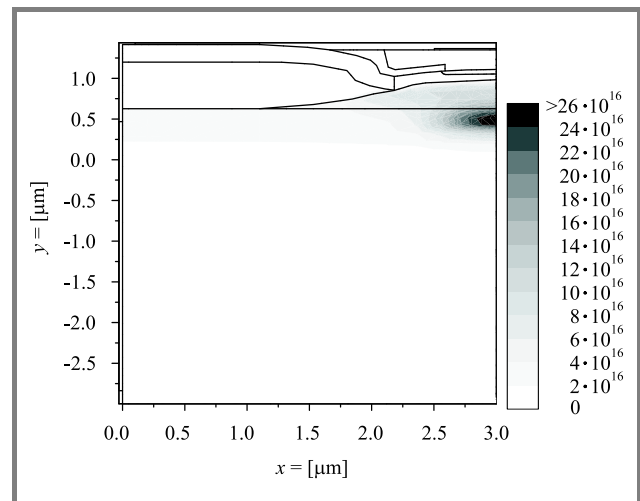
### 4.1. Device fabrication and process simulation

The devices under investigation are polysilicon-emitter double-base SiGe HBTs epitaxially grown by a chemical vapor deposition process. An implanted n-well, similar to the one used in the standard CMOS technology, is used. The buried layer is connected to a sinker to conduct the electron current from the buried layer to the collector contact. The base consists of an intrinsic base (below the emitter window) and an extrinsic base. The germanium content has a triangular shape. The base-emitter junction is formed by rapid thermal processing which causes out-diffusion of arsenic from the polysilicon emitter layer into the crystalline silicon.

The process simulation with DIOS [8] starts from the blank wafer to the final device and reflects real device fabrication as accurately as possible. The implant profiles as well as annealing steps are calibrated to one-dimensional SIMS profiles. To save computational resources the simulation domain covers only one half of the real device which is symmetric and the collector-sinker is not included in the structure.

### 4.2. SiGe HBT from the $0.8\ \mu\text{m}$ technology node

The influence of the selectively-implanted-collector (SIC) doping on device performance was studied in order to obtain an optimal profile for specific requirements (high speed or high breakdown voltage). For that purpose, four SiGe HBT structures with emitter areas of  $6 \times 0.8\ \mu\text{m}^2$  have been investigated both experimentally and by means of process simulation, followed by two-dimensional device simulation. The simulated device structure with the phosphorus SIC implant is shown in Fig. 7.



**Fig. 7.** Simulated device structure ( $0.8\ \mu\text{m}$  technology) and phosphorus collector implant [ $\text{cm}^{-3}$ ].

The only process step in which the four HBTs (hereafter referred to as dev. 1, dev. 2, dev. 3, dev. 4) differ is the combination of energy and dose used for the SIC implants, as summarized in Table 4. The resulting phosphorus doping profiles in vertical cuts under the emitter windows of the four devices are shown in Fig. 8.

Table 4  
Summary of key process and device parameters

Device	Energy [keV]	Dose [ $\text{cm}^{-2}$ ]	$f_T$ [GHz]	$\text{BV}_{\text{CE0}}$ [V]	$f_T \cdot \text{BV}_{\text{CE0}}$ [GHz · V]
Dev. 1	480	$7 \cdot 10^{12}$	32	4.0	128
Dev. 2	480	$3 \cdot 10^{13}$	40	3.7	148
Dev. 3	300	$7 \cdot 10^{12}$	33	3.1	102
Dev. 4	300	$3 \cdot 10^{13}$	42	2.3	97

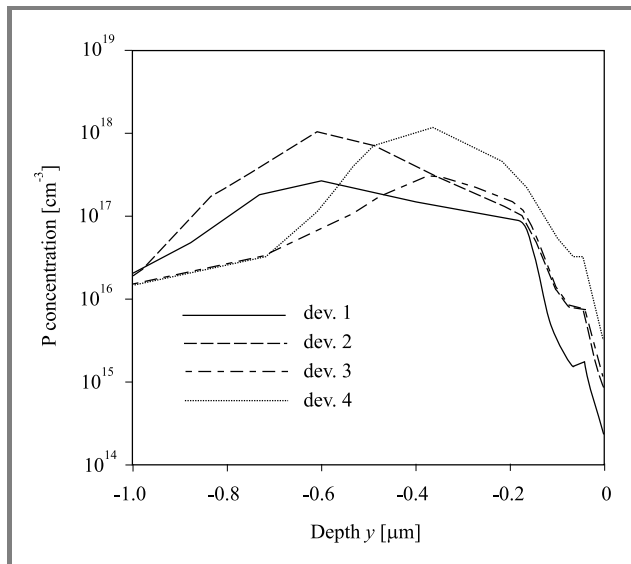


Fig. 8. Phosphorus doping profile under the emitter contact for all four devices.

A comparative Monte Carlo simulation of ion implantation [48] of phosphorus in silicon and SiGe was performed to check the accuracy of the process simulation with respect to SiGe (Fig. 9).

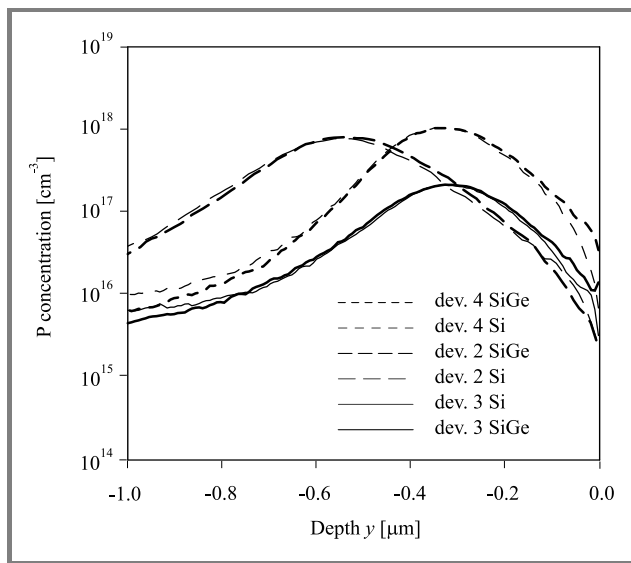


Fig. 9. Comparative simulation of Monte Carlo ion implantation of phosphorus in Si and SiGe.

The physical models in Minimos-NT are well calibrated [49]. The same is true for DESSIS, used for comparison. Both device simulators correctly reproduce the measured forward Gummel plot at 300 K (Fig. 10) with default models. The slight increase of collector current  $I_C$  with dose and energy at high bias is due to the differences in the base push-out effect.  $f_T$  is extracted by small-signal AC-analysis.

The only fitting parameters used in the simulation are the contribution of bandgap narrowing to the conduction band (here about 80% and 20% for donor and ac-

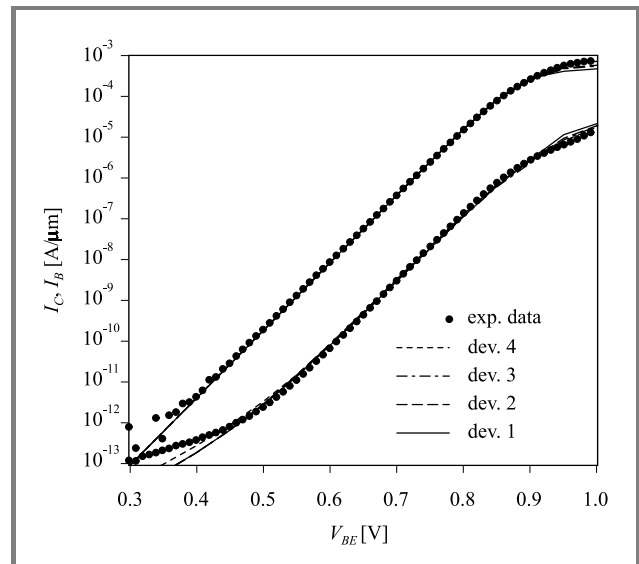


Fig. 10. Forward Gummel plots at  $V_{CB} = 0$  V. Comparison between measurement and simulation.

ceptor doping, respectively), and the concentration of traps in the Shockley-Read-Hall recombination model (here 10<sup>13</sup> cm<sup>-3</sup>).

However, as can be seen in Figs. 11 and 12, both DESSIS and Minimos-NT failed to explain the experimentally observed similarity in peak  $f_T$  for dev. 1 and dev. 3 and, respectively, for dev. 2 and dev. 4. This again turned our attention to the SIC implant. An automated device calibration with our TCAD framework [50] was performed. It turned out that 50% more phosphorus in the collector of the two low-dose devices (dev. 1 and dev. 3) already gives an acceptable qualitative agreement.

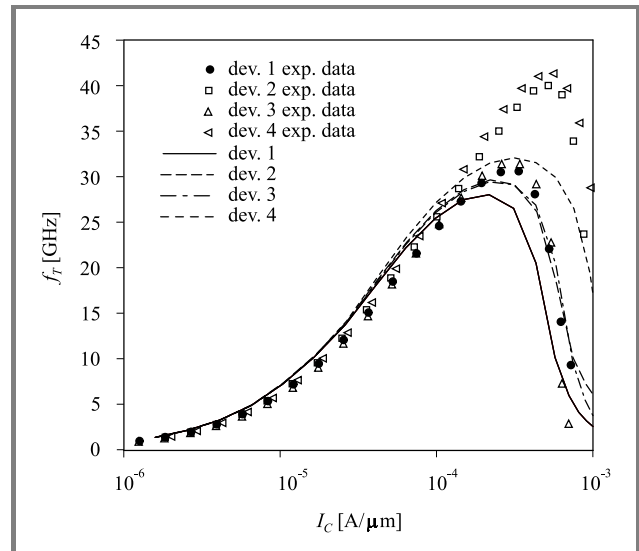
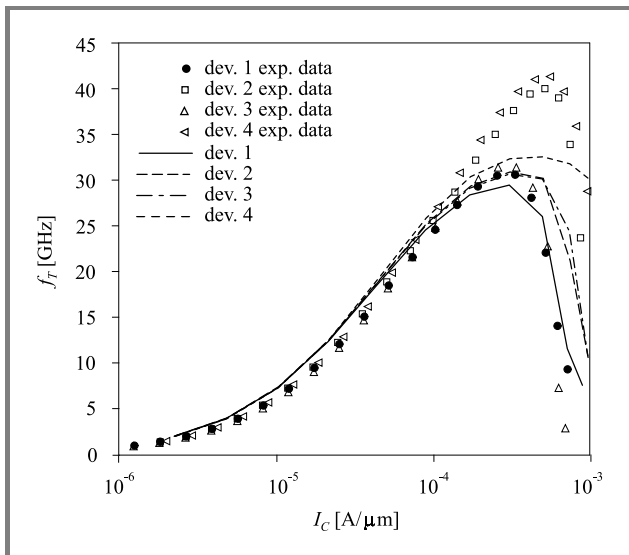
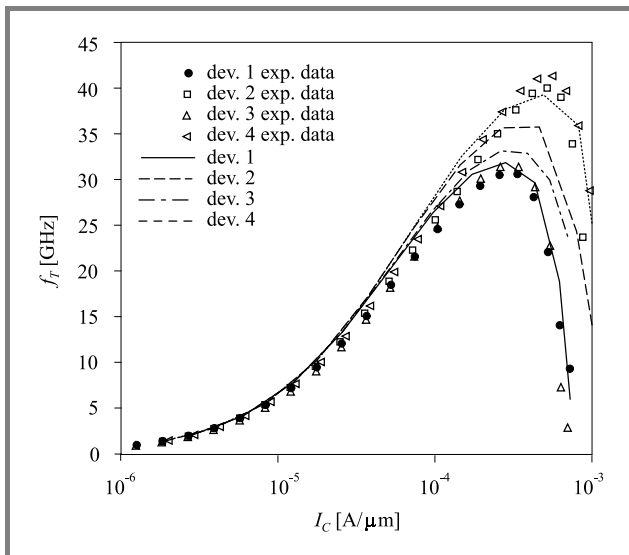


Fig. 11. Frequency  $f_T$  versus  $I_C$  at  $V_{CE} = 1.5$  V. Comparison between measurement and drift-diffusion simulation with DESSIS.

It is known that with shrinking device dimensions non-local effects, such as velocity overshoot, become more pronounced. Neglecting these effects can be a reason for un-

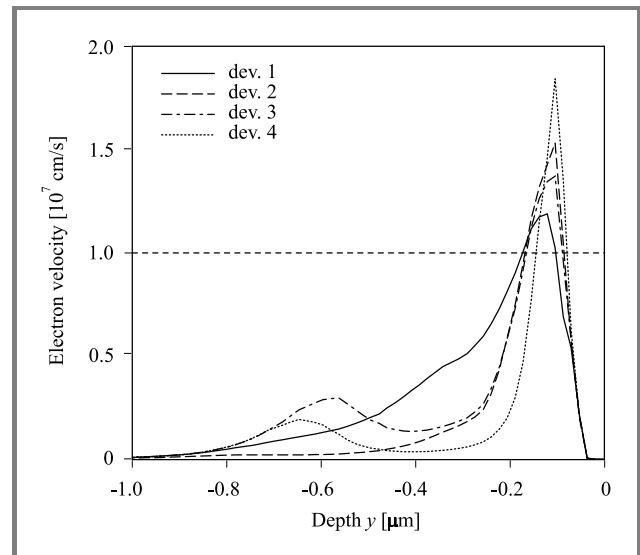


**Fig. 12.** Frequency  $f_T$  versus  $I_C$  at  $V_{CE} = 1.5$  V. Comparison between measurement and drift-diffusion simulation with Minimos-NT.

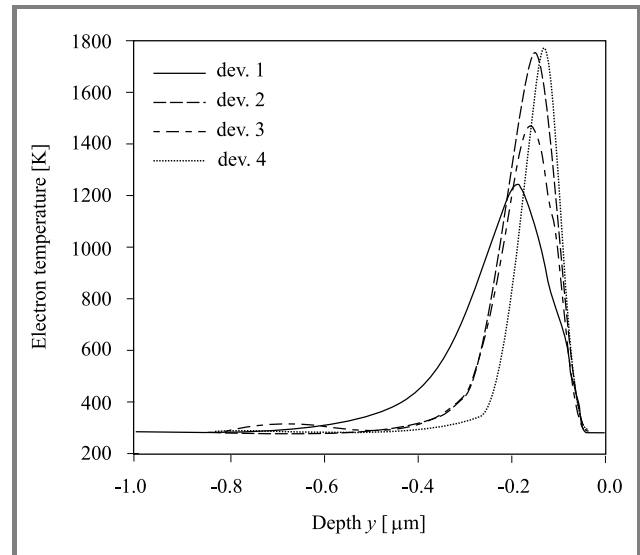


**Fig. 13.** Frequency  $f_T$  versus  $I_C$  at  $V_{CE} = 1.5$  V. Comparison between measurement and hydrodynamic simulation with Minimos-NT.

derestimating  $f_T$  [51]. For that purpose, we performed simulations with the hydrodynamic transport model which improved the results quantitatively (Fig. 13). Figure 14 shows the velocity overshoot over the greater part of the base region which is about twice the saturation velocity limit in the drift-diffusion case ( $10^7$  cm/s). This correlates to the higher electron energy (Fig. 15) in the collector and explains the increase of  $f_T$  in comparison to drift-diffusion simulations (see Figs. 11 and 12). The good agreement at low currents is very important since HBTs typically operate at much lower frequencies than at the maximum  $f_T$ . Simulations prove that in this range optimizations of the SIC implant do not have the influence on  $f_T$ , i.e. the base-emitter capacitance and not the base-collector capac-



**Fig. 14.** Electron velocity overshoot in the base-collector space charge region at  $V_{CE} = V_{BE} = 0.88$  V.



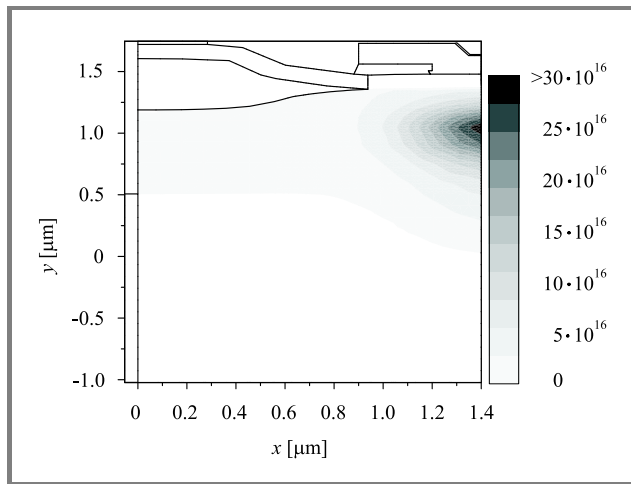
**Fig. 15.** Electron temperature distribution in the four simulated devices at  $V_{CE} = V_{BE} = 0.88$  V.

itance is dominating. The maximum  $f_T$  was found to have a stronger dependence on the dose than on the energy of the implants.

Furthermore, the important figure of merit  $BV_{CE0} \cdot f_T$  (see Table 4) reaches a maximum for high SIC implant energies (deep implant) and high SIC doses. We found that the higher  $f_T$  for high-dose/low-energy SIC implants is due to a smaller base width and a delayed onset of the base push-out effect due to the higher collector doping.

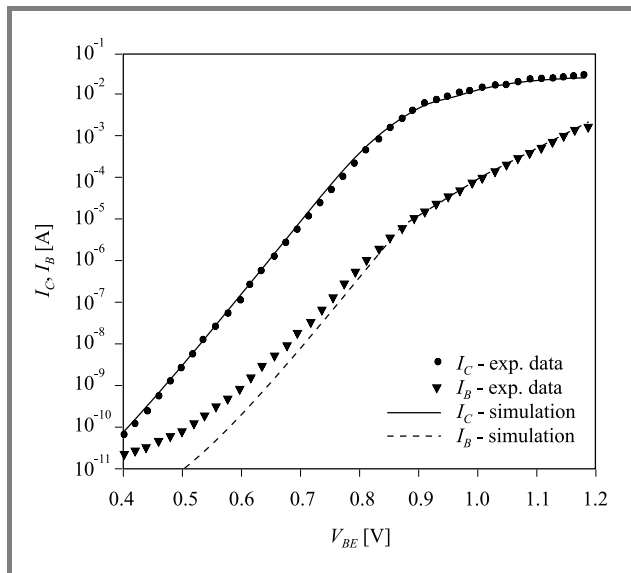
#### 4.3. SiGe HBT from the 0.35 $\mu\text{m}$ technology node

The investigated SiGe HBTs from the next generation have emitter areas of  $12 \cdot 0.4 \mu\text{m}^2$ . The device structure with the phosphorus SIC implant is shown in Fig. 16.



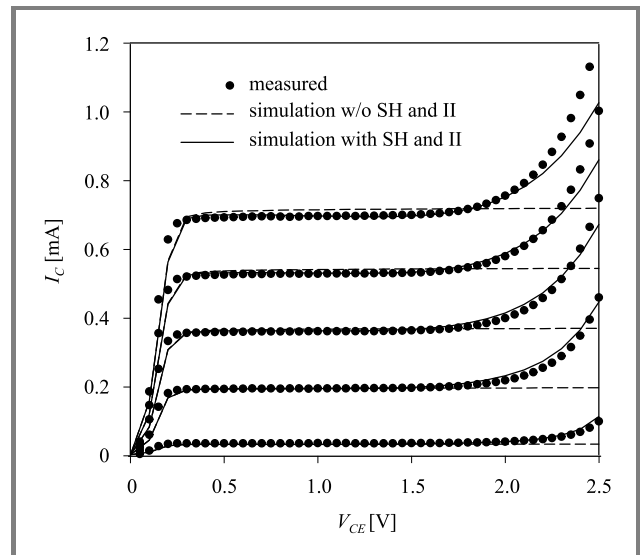
**Fig. 16.** Simulated device structure (0.35 μm technology) and phosphorus collector implant [cm⁻³].

All important physical effects, such as surface recombination, impact ionization (II) generation, and self-heating (SH), are properly modeled and accounted for in the simulation in order to get good agreement with the measured forward (Fig. 17) and output characteristics (Fig. 18) using a concise set of models and parameters. In contrast, simulation without including SH effects cannot reproduce the experimental data, especially at high power levels. The only fitting parameters used in the simulation are the contribution of BGN to the conduction band, the trap charge density in the Shockley-Read-Hall recombination model (here 10¹⁴ cm⁻³), the velocity recombination for holes in the polysilicon contact model [52] used at the emitter contact, and the substrate thermal resistance.



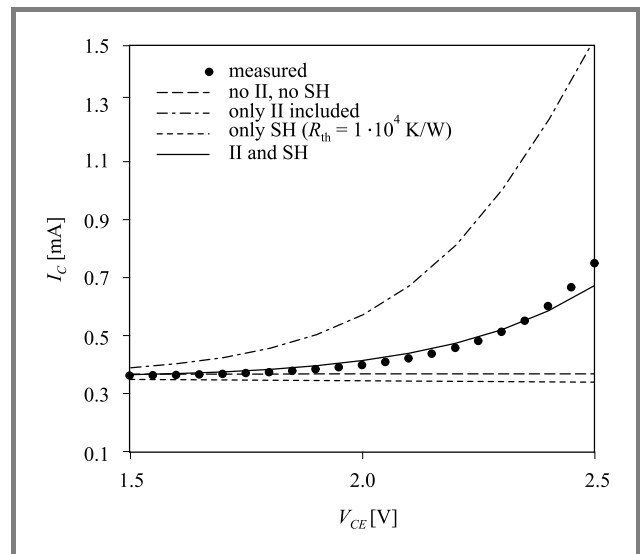
**Fig. 17.** Forward Gummel plots at V\_CB = 0 V: comparison between measurement data and simulation at room temperature.

A closer look at the increasing collector current I\_C at high collector-to-emitter voltages V\_CE and constant base current I\_B, stepped by 0.4 μA from 0.1 μA to 1.7 μA, reveals



**Fig. 18.** Output characteristics: simulation with and without self-heating (SH) and impact ionization (II) compared to measurement data. I\_B is stepped by 0.4 μA from 0.1 μA to 1.7 μA.

the interplay between self-heating and impact ionization (Fig. 19). While impact ionization leads to a strong increase of I\_C, self-heating decreases it. In fact, both I\_C and I\_B increase due to self-heating at a given bias condition. As the change is relatively higher for I\_B, in order to maintain it at the same level, V\_BE and, therefore, I\_C decrease.



**Fig. 19.** Output characteristics for I\_B = 0.9 μA: a closer look at the increasing I\_C at high V\_CE reveals the interplay between self-heating (SH) effect and impact ionization (II) generation.

A proper DC calibration is an important prerequisite for AC simulation (Fig. 17) Note that it is absolutely necessary for AC simulations to take the complete device structure into account in order to consider the capacitances between collector and substrate C\_CS as well as between base and collector C\_BC.



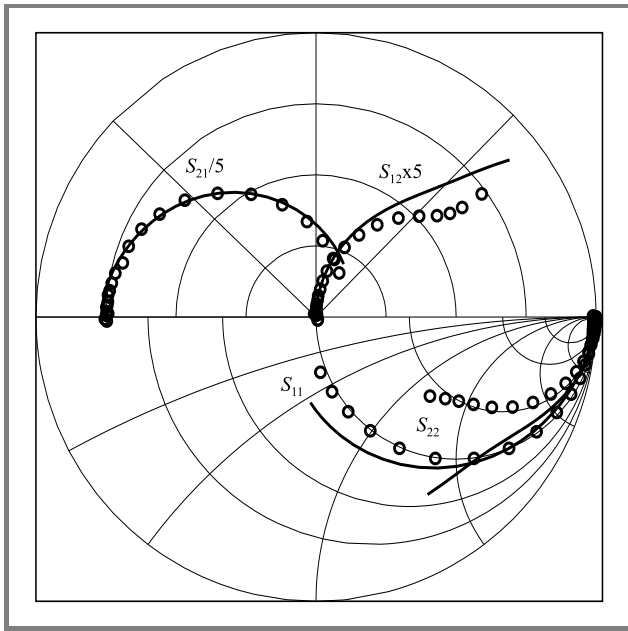


Fig. 20.  $S$ -parameters in a combined Smith chart (radius = 1) from 50 MHz to 31 GHz at  $V_{CE} = 1$  V and current density  $J_C = 28$  kA/cm<sup>2</sup> (measurements with circles).

The quality of the simulated (intrinsic)  $Y$ -parameters is proven by calculating the row and column sums of the admittance matrix, which have to be zero according to Kirchhoff's laws. The simulation yields errors of about  $10^{-16}$  A/V for typical matrix entries of  $10^{-3}$  A/V. The transformation to intrinsic  $S$ -parameters is completely analytical and, thus, the results can be directly compared to the measurement data. Since the measurement environment accounts for the parasitics, no transformation to extrinsic parameters is necessary.

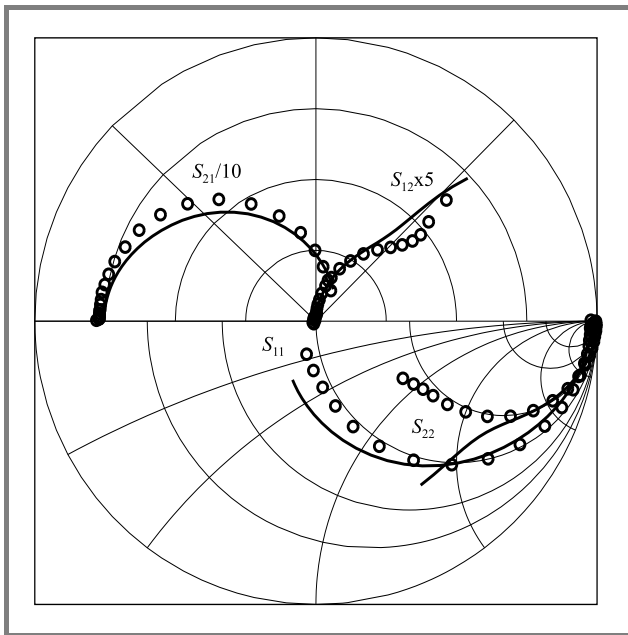


Fig. 21.  $S$ -parameters in a combined Smith chart (radius = 1) from 50 MHz to 31 GHz at  $V_{CE} = 1$  V and current density  $J_C = 76$  kA/cm<sup>2</sup> (measurements with circles).

Figures 20 and 21 show a comparison of simulated and measured  $S$ -parameters at  $V_{CE} = 1$  V and current densities  $J_C = 28$  kA/cm<sup>2</sup> and  $J_C = 76$  kA/cm<sup>2</sup> in the frequency range between 50 MHz and 31 GHz. For the same device we calculated the matched gain  $g_m$  and the short-circuit current gain  $h_{21}$  in order to extract the figures of merit  $f_T$  and  $f_{max}$  found at the respective unity-gain points.

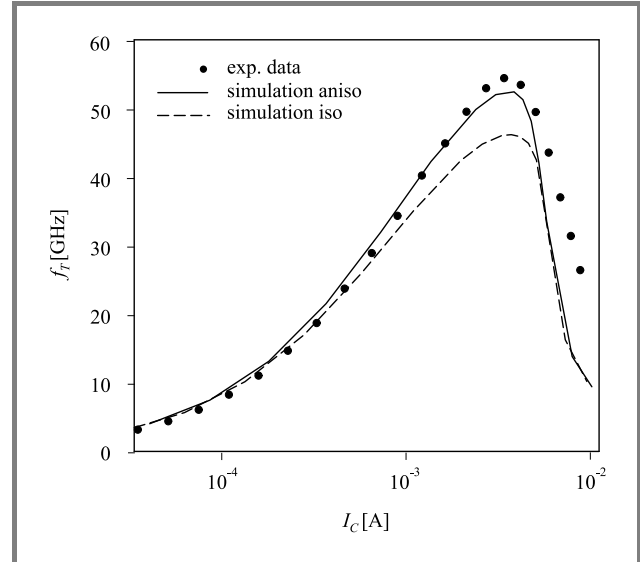


Fig. 22. Cut-off frequency  $f_T$  versus collector current  $I_C$  at  $V_{CE} = 1$  V (anisotropic with solid line, isotropic with dashed line, measurements with circles).

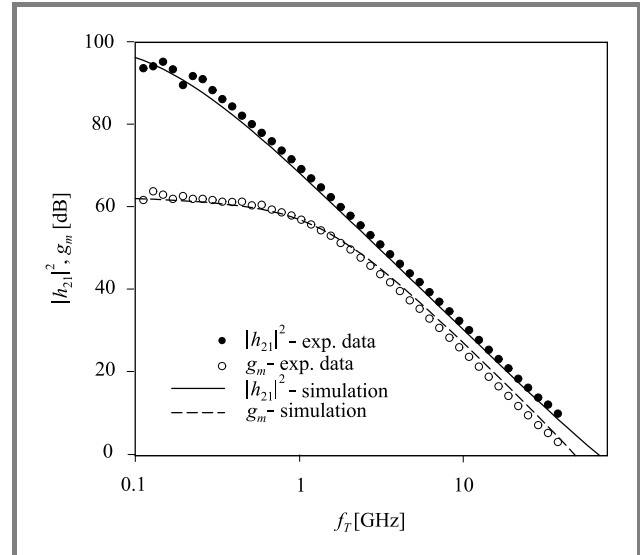


Fig. 23. Short-circuit current gain  $h_{21}$  and matched gain  $g_m$  versus frequency at  $V_{CE} = 1$  V and current density  $J_C = 76$  kA/cm<sup>2</sup> (measurements with circles).

Figures 22 and 23 show the comparison of our results and the corresponding measurement data. While the measurement covers a range up to 31 GHz the simulation is extended to frequencies beyond the unity-gain point. The peak of the  $f_T$ -curve in Fig. 22 corresponds exactly to the frequency at the respective intersection in Fig. 23. In ad-

dition, the effect of the introduction of anisotropic electron mobility is demonstrated in Fig. 22.

## 5. Conclusion

A brief overview of the state-of-the-art of simulation tools for SiGe HBTs has been given. Critical issues for numerical modeling of SiGe devices have been discussed including accurate models for bandgap narrowing and minority/majority electron mobility in strained SiGe. We have presented experiments and simulations of SiGe HBTs. Good agreement was achieved both with experimental DC-results (forward and output characteristics) and with high-frequency data. We were able to extract various sets of small-signal parameters as well as related figures of merit by means of simulation with Minimos-NT. The newly established models are beneficial for future process development.

## Acknowledgment

The authors acknowledge the ion implantation simulation from A. Hössinger and valuable inputs from G. Röhrer, S. Wagner, T. Grasser, and H. Kosina. The work is supported by the Austrian Science Fund (FWF), Project P14483-MAT, by CLPP BAS Center of Excellence in IT, by austriamicrosystems AG, Unterpremstätten, Austria, and by Infineon Technologies AG, Munich, Germany.

## References

- [1] J. Böck, H. Schäfer, H. Knapp, D. Zöschg, K. Aufinger, M. Wurzer, S. Boguth, M. Rest, R. Schreiter, R. Stengl, and T. Meister, "Sub 5 ps SiGe bipolar technology", *IEDM Tech. Dig.*, pp. 763–766, 2002.
- [2] J.-S. Rieh, B. Jagannathan, H. Chen, K. Schonenberg, D. Angell, A. Chinthakindi, J. Florkey, F. Golan, D. Greenberg, S.-J. Jeng, M. Khater, F. Pagette, C. Schnabel, P. Smith, A. Stricker, K. Volant, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "SiGe HBTs with cut-off frequency near 300 GHz", *IEDM Tech. Dig.*, pp. 771–774, 2002.
- [3] B. Jagannathan, M. Meghelli, A. V. Rylyakov, R. A. Groves, A. K. Chinthakindi, C. M. Schnabel, D. A. Ahlgren, G. G. Freemann, K. J. Stein, and S. Subbanna, "A 4.2-ps ECL ring-oscillator in a 285 GHz  $f_{max}$  SiGe technology", *IEEE Electron Dev. Lett.*, vol. 23, no. 9, pp. 541–543, 2002.
- [4] T. Hashimoto, Y. Nonaka, T. Saito, K. Sasahara, T. Tominari, K. Sakai, K. Tokunaga, T. Fujiwara, S. Wada, T. Udo, T. Jinbo, K. Washio, and H. Hosoe, "Integration of a 0.13- $\mu\text{m}$  CMOS and a high performance self-aligned SiGe HBT featuring low base resistance", *IEDM Tech. Dig.*, pp. 779–782, 2002.
- [5] APSYS, <http://www.crosslight.com/downloads/downloads.html>
- [6] ATLAS/Blaze, <http://www.silvaco.com/products/vwv/atlas/>
- [7] BIPOLE3, <http://www.bipsim.com/mainframe.html>
- [8] DESSIS and DIOS, <http://www.ise.com/products/index.html>
- [9] G-PISCES-2B, <http://www.gateway-modeling.com/products.htm>
- [10] MEDICI, [www.synopsys.com/products/avmrg/device\\_sim\\_ds.html](http://www.synopsys.com/products/avmrg/device_sim_ds.html)
- [11] E. Buturla, P. Cottrell, B. Grossman, and K. Salsburg, "Finite-element analysis of semiconductor devices: the FIELDAY program," <http://www.research.ibm.com/journal/rd/441/buturla.pdf>
- [12] NEMO, <http://www.cfdrc.com/nemo/>
- [13] PISCES-ET, <http://www-tcad.stanford.edu/tcad.html>
- [14] FLOODS and FLOOPS, <http://www.tec.ufl.edu/floods/>
- [15] C. Jungemann, B. Neinhüs, and B. Meinerzhagen, "Full-band Monte Carlo device simulation of a SiGe/Si HBT with a realistic Ge profile", *IEICE Trans. Electron.*, vol. E83-C, no. 8, pp. 1228–1234, 2000.
- [16] DEVICE, <http://www.uv.ruhr-uni-bochum.de/>
- [17] nextnano3, <http://www.webplexity.de/nextnano3.php>
- [18] J. Geßner, F. Schwierz, H. Mau, D. Nuernbergk, M. Roßberg, and D. Schipanski, "Simulation of the frequency limits of SiGe HBTs", in *Proc. Model. Simul. Microsyst.*, Puerto Rico, 1999, pp. 407–410.
- [19] Minimos-NT 2.0 User's Guide, Institut für Mikroelektronik, Technische Universität Wien, Austria, <http://www.iue.tuwien.ac.at/software/minimos-nt>
- [20] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Wien, New York: Springer, 1984.
- [21] W. Hänsch, *The Drift Diffusion Equation and its Application in MOSFET Modeling*. Wien, New York: Springer, 1991.
- [22] C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation*. Wien, New York: Springer, 1989.
- [23] K. Hess, Ed., *Monte Carlo Device Simulation: Full Band and Beyond*. Boston, Dordrecht, London: Kluwer, 1991.
- [24] H. Kosina and S. Selberherr, "A hybrid device simulator that combines Monte Carlo and drift-diffusion analysis", *IEEE Trans. Comput. Aid. Des.*, vol. 13, no. 2, pp. 201–210, 1994.
- [25] W. Engl, A. Emunds, B. Meinerzhagen, H. Peifer, and T. Thoma, "Bridging the gap between the hydrodynamic and the Monte Carlo model – an attempt", in *Proc. VLSI Process./Dev. Model. Worksh.*, Osaka, 1989, pp. 32–33.
- [26] S. Laux and M. Fischetti, "The DAMOCLES Monte Carlo device simulation program", in *Computational Electronics*, K. Hess, J. Leburton, and U. Ravaioli, Eds. Kluwer, 1991, pp. 87–92.
- [27] W. Hänsch, T. Vogelsang, R. Kircher, and M. Orlowski, "Carrier transport near the Si/SiO<sub>2</sub> interface of a MOSFET", *Solid State Electron.*, vol. 32, no. 10, pp. 839–849, 1989.
- [28] K. Dragosits, V. Palankovski, and S. Selberherr, "Two-dimensional modeling of quantum mechanical effects in ultra-short CMOS devices", in *Advances in Simulation, Systems Theory and Systems Engineering*, N. Mastrokakis, V. Kluev, and D. Koruga, Eds. WSEAS Press, 2002, pp. 113–116.
- [29] D. Richey, J. Cressler, and A. Joseph, "Scaling issues and Ge profile optimization in advanced UHV/CVD SiGe HBT's", *IEEE Trans. Electron Dev.*, vol. 44, no. 3, pp. 431–440, 1997.
- [30] B. Gonzales, V. Palankovski, H. Kosina, A. Hernandez, and S. Selberherr, "An energy relaxation time model for device simulation", *Solid State Electron.*, vol. 43, pp. 1791–1795, 1999.
- [31] R. Quay, C. Moglestue, V. Palankovski, and S. Selberherr, "A temperature dependent model for the saturation velocity in semiconductor materials", *Mat. Sci. Semicond. Process.*, vol. 3, no. 1–2, pp. 149–155, 2000.
- [32] V. Palankovski and S. Selberherr, "Thermal models for semiconductor device simulation", in *Proc. Eur. Conf. High Temper. Electron.*, Berlin, 1999, pp. 25–28.
- [33] R. Quay, R. Reuter, V. Palankovski, and S. Selberherr, "S-parameter simulation of RF-HEMTs", in *Proc. High Perform. Electron Dev. Microw. Opt. Appl. EDMO*, Manchester, 1998, pp. 13–18.
- [34] S. Wagner, V. Palankovski, T. Grasser, R. Schultheis, and S. Selberherr, "Small-signal analysis and direct S-parameter extraction", in *Proc. Int. Symp. Electron Dev. Microw. Opt. Appl. EDMO*, Manchester, 2002, pp. 50–55.
- [35] J. Eberhardt and E. Kasper, "Bandgap narrowing in strained SiGe on the basis of electrical measurements on Si/SiGe/Si hetero bipolar transistors", *Mat. Sci. Eng.*, vol. B89, pp. 93–96, 2002.
- [36] Y. Varshni, "Temperature dependence of the energy gap in semiconductors", *Physica*, vol. 34, pp. 149–154, 1967.
- [37] S. Jain, *Germanium-Silicon Strained Layers and Heterostructures*, vol. 24 of *Advances in Electronics and Electron Physics*. Academic Press, 1994.

- [38] V. Palankovski, G. Kaiblinger-Grujin, and S. Selberherr, "Implications of dopant-dependent low-field mobility and band gap narrowing on the bipolar device performance", *J. Phys. IV*, vol. 8, pp. 91–94, 1998.
- [39] S. Jain and D. Roulston, "A simple expression for band gap narrowing (BGN) in heavily doped Si, Ge, GaAs and  $\text{Ge}_x\text{Si}_{1-x}$  strained layers", *Solid State Electron.*, vol. 34, no. 5, pp. 453–465, 1991.
- [40] Ž. Matutinović-Krstelj, V. Venkataraman, E. Prinz, J. Sturm, and C. W. Magee, "A comprehensive study of lateral and vertical current transport in  $\text{Si}/\text{Si}_{1-x}\text{Ge}_x/\text{Si}$  HBT's", *IEDM Tech. Dig.*, pp. 87–90, 1993.
- [41] M. Libezny, S. Jain, J. Poortmans, M. Caymax, J. Nijs, R. Mertens, K. Werner, and P. Balk, "Photoluminescence determination of the Fermi energy in heavily doped strained  $\text{Si}_{1-x}\text{Ge}_x$  layers", *Appl. Phys. Lett.*, vol. 64, no. 15, pp. 1953–1955, 1994.
- [42] G. Masetti, M. Severi, and S. Solmi, "Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus- and boron-doped silicon", *IEEE Trans. Electron Dev.*, vol. ED-30, no. 7, pp. 764–769, 1983.
- [43] K. Wolfstirn, "Hole and electron mobilities in doped silicon from radiochemical and conductivity measurements", *J. Phys. Chem. Solids*, vol. 16, pp. 279–284, 1960.
- [44] S. E. Swirhun, D. E. Kane, and R. M. Swanson, "Measurements of electron lifetime, electron mobility and band-gap narrowing in heavily doped p-type silicon", *IEDM Tech. Dig.*, pp. 24–27, 1986.
- [45] I. Y. Leu and A. Neugroschel, "Minority-carrier transport parameters in heavily doped p-type silicon at 296 and 77 K", *IEEE Trans. Electron Dev.*, vol. 40, no. 10, pp. 1872–1875, 1993.
- [46] S. Smirnov, H. Kosina, and S. Selberherr, "Investigation of the electron mobility in strained  $\text{Si}_{1-x}\text{Ge}_x$  at high Ge composition", in *Proc. Simul. Semicond. Process. Dev.*, pp. 29–32, 2002.
- [47] H. Kosina and G. Kaiblinger-Grujin, "Ionized-impurity scattering of majority electrons in silicon", *Solid State Electron.*, vol. 42, no. 3, pp. 331–338, 1998.
- [48] A. Hössinger and S. Selberherr, "Accurate three-dimensional simulation of damage caused by ion implantation", in *Proc. Model. Simul. Microsyst.*, Puerto Rico, 1999, pp. 363–366.
- [49] S. Selberherr, W. Hänsch, M. Seavey, and J. Slotboom, "The evolution of the MINIMOS mobility model", *Solid State Electron.*, vol. 33, no. 11, pp. 1425–1436, 1990.
- [50] T. Grasser, R. Strasser, M. Knaipp, K. Tsuneno, H. Masuda, and S. Selberherr, "Device simulator calibration for quartermicron CMOS devices", in *Proc. Simul. Semicond. Process. Dev.*, K. De Meyer and S. Biesemans, Eds., Leuven, 1998, pp. 93–96.
- [51] C. Jungemann, B. Neinhüs, and B. Meinerzhagen, "Comparative study of electron transit times evaluated by DD, HD, and MC device simulation for a SiGe HBT", *IEEE Trans. Electron Dev.*, vol. 48, no. 10, pp. 2216–2220, 2001.
- [52] Z. Yu, B. Ricco, and R. Dutton, "A comprehensive analytical and numerical model of polysilicon emitter contacts in bipolar transistors", *IEEE Trans. Electron Dev.*, vol. 31, no. 6, pp. 773–784, 1984.



**Vassil Palankovski** was born in Sofia, Bulgaria, in 1969. He received the diploma degree in electronics from the Technical University of Sofia in 1993. Afterwards he worked in the telecommunications field for three years. He joined the Institut für Mikroelektronik at the Technische Universität Wien in 1997, where he received the

doctoral degree in 2000, and is currently working as a post-doctoral researcher. In summer 2000 Dr. Palankovski held a visiting research position at LSI Logic Corp., Milpitas, California. His scientific interests include device and circuit simulation, heterostructure device modeling, and physical aspects in general.

e-mail: Palankovski@iue.tuwien.ac.at

Institute for Microelectronics, TU Vienna

Gusshausstr. 27–29, A-1040 Vienna, Austria



**Siegfried Selberherr** (IEEE Fellow) was born in Klosterneuburg, Austria, in 1955. He received the degree of diplomingenieur in electrical engineering and the doctoral degree in technical sciences from the Technische Universität Wien in 1978 and 1981, respectively. Dr. Selberherr has been holding the *venia docendi* on computer-

aided design since 1984. Since 1988 he has been the head of the Institut für Mikroelektronik and since 1999 he is dean of the Fakultät für Elektrotechnik und Informationstechnik at the Technische Universität Wien, Austria. His current topics are modeling and simulation of problems for microelectronics engineering.

e-mail: Selberherr@iue.tuwien.ac.at

Institute for Microelectronics, TU Vienna

Gusshausstr. 27–29, A-1040 Vienna, Austria