*Invited paper*

# Process and device requirements for mixed-signal integrated circuits in broadband networking

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**Abstract — The paper describes the present status of the broadband wireline infrastructure consisting of the backbone core, metro rings, access network, local and storage area networks. Examples of various mixed-signal integrated circuits are described. Based on these considerations required process and device performance is extrapolated.**

***Keywords — CMOS, SiGe, InP, networking, WAN, MAN, SAN, LAN, OEO conversion, cut-off frequency, manufacturability.***

## 1. Introduction – broadband network today

The convergence of voice, data and video onto a single network combined with large global consumer and corporate appetite for internetworking is leading to installation and upgrading of communication infrastructure worldwide. The paper reviews recent trends in broadband infrastructure deployment and shows future possible directions. Networking integrated circuits (ICs), being the nuts and bolts of this infrastructure build-up, are continuously evolving leading to very complex electronic devices. The main theme of the paper is to link dramatic changes in Internet network with demands placed on IC design, IC processes and device performance that are needed in order to continue fuelling this infrastructure growth.

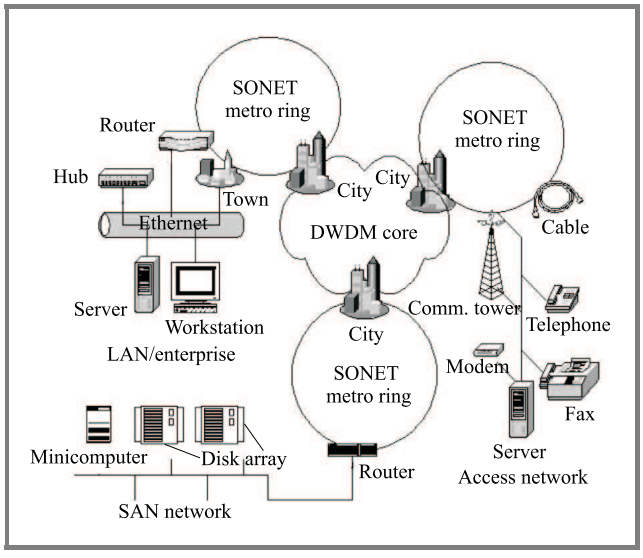


*Fig. 1.* Conceptual drawing of the broadband network.

The complexity of today's global network infrastructure has been primarily caused by the use of multiple networks, as shown in Fig. 1, and multiple protocols:

- Access networks – networks for both consumers and corporate customers to provide data, video and voice to all required locations using time-domain multiplexing (TDM), synchronous optical network (SONET), and asynchronous transfer mode (ATM) [1].
- LANs – local area networks that connect PCs, workstations, printers and other devices inside a building or campus, traditionally using Ethernet (10 Mbit/s, 100 Mbit/s and 1 Gbit/s) connections.
- SANs – storage area networks that connect backend storage disks via high-speed interfaces using primarily fiber channel (1 Gbit/s and 2 Gbit/s) protocols.
- MANs – metropolitan area networks that connect data and voice traffic at the city level typically using SONET rings (OC-48/OC-192[1]).
- WANs (core, backbone) – wide area networks which connect multiple corporate locations or cities across long distances. ATM, SONET and IP are used in the core of the network [2].

**Access**. Access networks need to carry both voice and data. Voice is carried using well-known circuit-switching techniques. Data is carried using multiple different technologies like TDM, integrated services digital network (ISDN), ATM, plesio-synchronous digital hierarchy (PDH), frame relay or digital subscriber loop (DSL). As data needs to be merged with voice at some point in the network, ATM is well suited for that purpose, being able to transport reliably voice over SONET (fiber) or over DSL (copper wire).

The access networks use different media for data transmission: copper twisted pair wires, coaxial cables, optical fibers or simply air in the case of wireless access. Digital subscriber loop technology is becoming the dominant technology for the transmission over the copper wire, while cable modems are used for transmission over

[1]OC in SONET indicates optical carrier rate. The bandwidth of OC-48 is 2.488 Gbit/s while that of OC-192 is 9.953 Gbit/s.

the coaxial cable. As very small percentage of businesses and households has a direct fiber connection, fiber to the home (FTTH) technology cannot be effectively deployed. Instead, fiber to the curb (FTTC) is being considered due to the progress in passive optical networks (PON) technology which uses passive optical splitters to split the optical signal from fiber to copper wires.

**Enterprise**. Ethernet rules local area networks. This well known technology has managed to evolve from 10 Mbit/s to 100 Mbit/s (fast Ethernet) to 1 Gbit/s (gigabit Ethernet), and now to 10 Gbit/s, in a backwards compatible fashion. Ethernet architects are already discussing 40 and 100 Gbit/s versions of this technology although practical implementations are probably years away. Due its popularity and massive deployment in LANs, Ethernet is cheap. As a result it threatens other protocols in areas outside LAN. In particular, optical Ethernet (running Ethernet over optical fiber) might become popular in the future in the access and metro networks shunning away ATM and SONET.

**Storage**. Storage area networking is currently the fastest growing segment of broadband deployment. While discussions continue on merits of network attached storage (NAS) vs. storage area networks, both remain universally deployed in large and very large corporations to store massive amounts of corporate data. Fiber channel is the dominant protocol in SANs although iSCSI[2] implementations might threaten that dominant position in the future.

**Metro**. Current metropolitan infrastructure is primarily based on SONET rings that carry ATM and IP traffic [3, 4]. Future services might use various other technologies, such as next-generation SONET, optical Ethernet, multi-service dense wavelength division multiplexing (DWDM), or multi protocol Lambda switching (MPLS) [5, 6]. It needs to be pointed out that the important function of metropolitan area networks is also to collect wireless data traffic from third generation (3G) wireless networks.

**Core**. Core networks require transmission over long distances, typically beyond 500 km, preferably beyond 5000 km. In traditional networks repeaters are used to regenerate signals every 60–80 km [7, 8]. Long span without repeaters can be also accomplished using optical amplification enhanced by pulse shaping and error coding techniques. Optical signals can be restored using Raman or erbium doped fiber amplifiers (EDFAs). Future optical techniques of ultra-long haul systems might use solitons, which, due to their unique properties, can travel in optical fiber over very long distances. It is also anticipated that optical switching technology, probably based on MEMs structures, will replace electronic switching in the core of the network [9].

[2]iSCSI is a new technology of running IP Internet Protocol over small computer system interface (SCSI) protocol.

## 2. Mixed-signal integrated circuits for broadband communication

Broadband communication ICs are semiconductor chips that enable processing and transmission of voice, video and data, in either electrical or optical form, from one location to another across broadband Internet network.

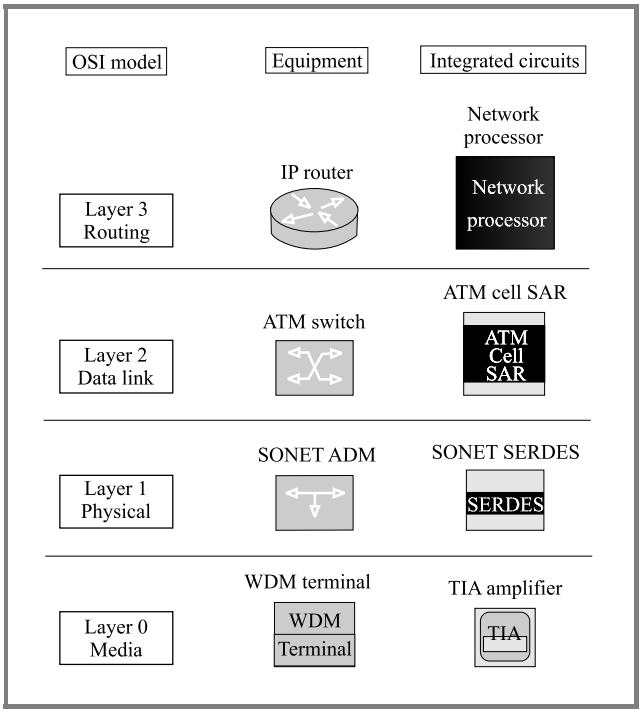


***Fig. 2.*** Classification of integrated circuits (right), networking equipment (middle) using open interconnect system (OSI) model (left).

Figure 2 summarizes the classification of integrated circuits in broadband networking. The left column shows open system interconnect (OSI) model hierarchy consisting of the following layers:

- Layer 0 or media layer. An example of networking technology is wavelength division multiplexing (WDM), an example of networking equipment is a WDM terminal, and an example of an integrated circuit is trans-impedance amplifier (TIA).
- Layer 1 or physical layer. An example of networking technology is SONET transport, an example of networking equipment is SONET add/drop multiplexer (ADM), and an example of an integrated circuit is SONET SERDES[3].
- Layer 2 or data link layer. An example of networking technology is ATM, an example of networking equipment is ATM switch, and an example of an

[3]SERDES – to SERialize and DE-Serialize. MUX/DE-MUX type IC device that converts parralel data stream into a serial one.

integrated circuit is ATM cell segmentation and reassembly (SAR) device.

- Layer 3 or networking layer. An example of networking technology is IP routing, an example of networking equipment is a core router, while an example of an integrated circuit is network processor.

After OSI model has been introduced and networking equipment has been broadly classified, we can discuss the role of integrated circuits in the networking gear. Integrated circuits typically perform the following functions:

- Coding, modulation, and amplification of electrical signals for transmission through physical medium (optical fiber, twisted pair copper wire, coaxial cable). Also in reverse direction: de-coding, demodulation and equalization for reception of electrical signals. These devices are typically referred to as physical medium devices (PMDs) and physical layer devices (PHYs), and are considered to be Layer 1 devices in the OSI protocol stack. These devices are either completely analog or mixed-signal with significant analog content.
- Data formatting into frames or cells using predefined protocols (ATM, Ethernet, fiber channel, etc.). These devices are typically referred to as framers or mappers, and are considered to be Layer 2 devices. These devices are providing digital processing and the only analog/mixed-signal circuitry they require is high-speed serial links used for chip-to-chip communication.
- Data-packet processing. Processing functions include protocol conversion, packet forwarding, policing, look-up, classification, encryption, and traffic management [10–12]. These devices are typically referred to as network processors, classification engines or traffic managers, and are considered to be Layer 3 devices. Typically they are purely digital devices that use highly parallel I/O interfaces.

### *2.1. PMD and PHY mixed-signal devices*

In general, physical medium dependent devices are being used for I/O interfacing to physical media, like fiber, copper wire or coaxial cable. Typically they are data protocol independent as they deal only with physical effects and electrical signals. PMDs include devices such as amplifiers for photo-detectors or drivers for lasers. PMD devices require analog design expertise.

Physical layer devices are responsible for defining how the traffic will be transported from one location to another. PHY devices include SONET SERDES blocks, clock and data recovery (CDR) circuits [14, 15], Ethernet transceivers [16], cable and xDSL modems chips [17, 18]. The most critical parameters for these devices are related to timing jitter. PHY devices have to comply with elaborate specification for the amount of jitter being generated (intrinsic jitter), the amount of jitter the device can tolerate at its input (jitter tolerance), and the transfer characteristics of the output jitter vs. applied input jitter (jitter transfer). Different jitter specifications exist for different transport technologies (SONET, Ethernet or fiber channel) making it difficult to implement the same phase-lock loop design in different devices.

### *2.2. Optical to electrical to optical conversion*

Most of network communication in wide area network is carried on optical fibers while most networking in local area networks relies on electronic devices and transport along electrical wires [13]. As a result, the optical to electrical to optical (O-E-O) conversion process is required in numerous places in the modern broadband network. We will use the O-E-O link example to illustrate further challenges in mixed-signal IC design. Figure 3 shows an optical module containing a number of PMD and PHY devices.

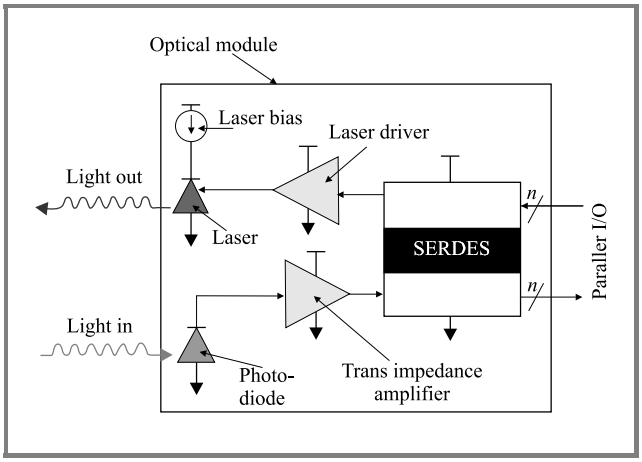


***Fig. 3.*** Optical module for O-E-O conversion containing optical devices (laser and photodiode), analog circuits (laser driver and trans-impedance amplifier), and the mixed-signal IC.

The optical signal is received by a photo-diode. Both PIN and avalanche photo diodes (APD) are used for that purpose. Since the photodiode produces photo-current I while most electronic devices require voltage signal V, the conversion from I to V is done by a PMD device called trans-impedance amplifier. While converting from current to voltage the amplifier also amplifies the signal. It is important to note that TIA is extremely noise sensitive, as it deals with very small currents in the range of a few pico amperes (pA). Due to this noise sensitivity TIA is the hardest element to integrate with other ICs in the optical module.

After an I-to-V conversion a voltage signal is ready for further processing. In some cases the amplitude of the signal coming out of the TIA is too small and requires additional amplification by the limiting amplifier (not shown

in Fig. 3), the output of which will provide constant signal amplitude regardless of the strength of the optical signal being converted. The limiting amplifier is another example of a PMD device.

The signal from the limiting amplifier is received by the clock and data recovery block inside SERDES IC. The CDR block recovers the clock from the NRZ data stream using analog phase-lock loop techniques. The jitter tolerance of a CDR is typically the most challenging parameter to be met in commercial products, because it has to comply with stringent networking standards[4]. After clock recovery, the signal needs to be de-serialized to lower rates. The circuitry that performs this function is called a de-multiplexer (de-mux) or de-serializer, and is also typically a part of the SERDES IC. Using the recovered clock and lower speed, further digital processing of the parallel data can be performed in a follow-up Layer 2 digital device.

Similar processing occurs in the reverse, egress direction. The data generated by a Layer 2 device is being serialized using a multiplexer (mux) or serializer device. Clock multiplication unit (CMU) is used to generate high purity reference clock for data transmission. The entire SERDES operation is summarized in Fig. 4.

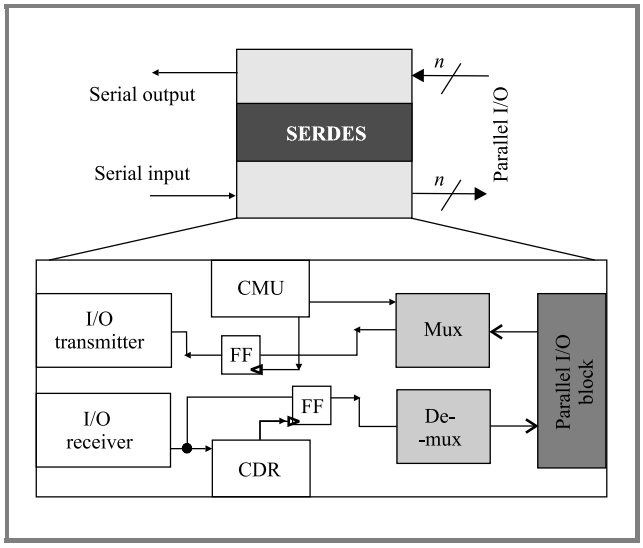


***Fig. 4.*** Schematic block diagram of SERDES IC device that incorporates analog I/O receive and transmit blocks, clock and data recovery (CDR), clock multiplication phase-locked loop (CMU), mux and de-mux, and parallel digital I/O block. FF indicates a flip flop, as two critical flip-flops are shown that are used to re-time the data in the transmit direction and clean up the receive data using the CDR supplied recovered-clock.

The data transmitted from SERDES reaches a PMD device called a laser driver. The laser driver in turn modulates the laser itself, effectively converting the electrical signal into an optical one.

A laser driver has to meet very specific requirements that are somewhat different from those imposed on other PMD components. It has to operate at the same high-date rate as other devices but it must deliver higher voltage swings as well. The requirement for higher voltage swing is due to currently available laser structures. For example, conventional Mach-Zehnder (MZ) or eletro-absorption (EA) structures require voltage swings of 5 V or more to achieve very good extinction ratio.

[4]Each networking protocol, like SONET or Ethernet, defines different criteria for jitter requirements.

## 3. Device requirements for broadband circuits

While the current broadband infrastructure runs at the rates of up to 10 Gbit/s, the future network will require processing at 40 Gbit/s and beyond [19, 20]. It is generally accepted that 40 Gbit/s data rates are currently in the realm of SiGe, GaAs or InP technologies due to their fundamental device properties (high mobility, transconductance and breakdown) [21]. However, for a given technology node, the mainstream CMOS technology shows potential competitive advantages in terms of cost, level of integration and power dissipation as technology scaling enables both increased functionality and speed (frequency) in integrated circuits. It is vital to predict at which point CMOS performance will be sufficient to produce 40 Gbit/s circuits.

Cut-off frequency $f_T$ is a critical parameter for transistor performance. It is defined as the frequency at which the transistor voltage gain becomes unity; $f_T$ is frequently used for speed comparison between various semiconductor processes. Figure 5 presents $f_T$ data for NMOS, PMOS and SiGe HBT transistors as a function of lithographic feature size [20].

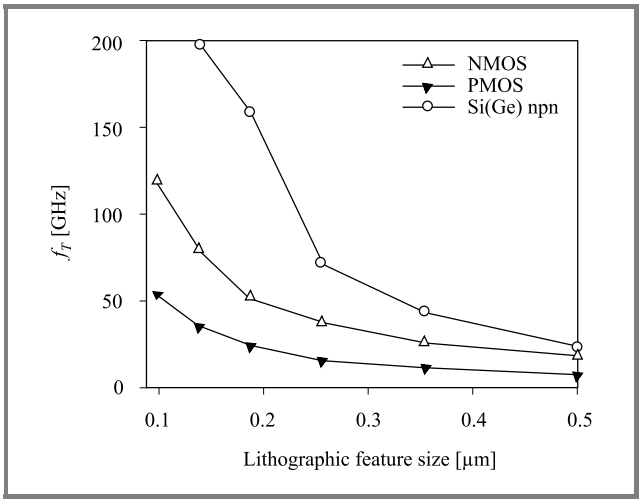


***Fig. 5.*** Cut-off frequency data as a function of lithographic feature size for NMOS, PMOS, and SiGe npn transistors.

The plots in Fig. 5 represent measured data up to 0.13 $\mu$m and simulation-based extrapolated data up to 90 nm. All MOSFET and SiGe HBT measured data represent maximum $f_T$ at the best possible bias point. For MOSFETs

the optimum bias point is: $V_{GS} = V_{DS} = V_{DD}$. For example, in a 0.13 $\mu$m NMOSFET at $V_{DS} = 0.4$ V and $V_{GS} = 0.65$ V (low bias) the measured $f_T$ is 70 GHz, while the maximum cut-off frequency is around 80 GHz. It is interesting to note that even at low bias MOSFET cut-off frequency is still higher than that of SiGe HBT biased at $V_{CE} = 0.4$ V.

Some interesting observations can be drawn from Fig. 5. First, NMOS device has a 2 $\times$ speed advantage over PMOS. This well-known result reminds us that all fast CMOS circuits will continue to rely on NMOS design in high-speed paths of operation using PMOS devices only for biasing and loading. Second, SiGe devices retain a 2 $\times$ speed advantage over NMOS transistors. Or, to put it in a different perspective, CMOS process is behind SiGe, typically by two generations.

It is instructive to compare the predictions of the International Technology Roadmap for Semiconductors (ITRS) with the measured data [20]. This comparison is presented in Table 1.

Table 1
Cut-off frequency versus process feature size*

| Process feature size [nm] | Cut-off frequency [GHz] ITRS 1999 | Cut-off frequency [GHz] ITRS 2001 | Cut-off frequency [GHz] data from Fig. 2 [20] |
|---|---|---|---|
| 180 | 20 | – | 50 |
| 150 | 25 | 132 | – |
| 130 | 30 | 149 | 80 |
| 90 | 40 | 225 | – |
| 65 | – | 371 | 120 |

* Data compiled from International Technology Roadmap for Semiconductors presented in 1999 and 2001. The data from reference [20] is included for comparison.

Clearly, the predictions made in 1999 were very pessimistic, while the subsequent correction in 2001 overly optimistic. In fact, a comparison between ITRS 1999 and ITRS 2001 indicates astonishing differences – the values predicted in 2001 are approximately 5 times higher than those predicted in 1999 for the same feature size.

## 4. Process requirements

In the recent years advanced CMOS processes could compete with early SiGe implementations as the cost of mask making was not a major economic factor. For example, 0.18 $\mu$m CMOS was competitive to 0.35 $\mu$m SiGe process by virtue of offering similar performance in a well-known CMOS design and process environment. This trend might change in the future as the cost of mask making rapidly increases with feature size reductions[5]. With non-recurring engineering charges (NRE) for mask making reaching over one million dollars for 90 nm CMOS process it will likely be more cost effective to manufacture ICs in 0.18 $\mu$m SiGe process rather than in 90 nm CMOS. Based on the cut-off frequency data presented in both processes one can expect similar high-frequency performance. The only application driving the 90 nm CMOS process option would be digital devices with extremely high (over 10 million) gate count.

The operation frequency of real circuits is lower than the pure device speed metrics because real circuits have to drive a heavy fan-out load in addition to device and interconnect parasitics. One popular circuit speed metric for high performance microprocessor design is the FO4 delay, where a CMOS inverter drives a load of fan-out of four. Although FO4 delay is a different parameter than $f_T$, both are very strongly correlated. For clarity we will continue to use the cut-off frequency $f_T$ as a measure of the speed of the process.

Without design innovations, the achievable operation frequency of circuits is around $f_T/10$. With some design innovations it is possible to design circuits up to $f_T/4$. In fact a review of the papers published in the *Journal of Solid-State Circuits* during the last 5 years indicates that state-of-the-art circuits have their frequency of operation somewhere between $f_T/10$ and $f_T/2$. However, it has to be pointed out that some of the circuits published in the literature are of academic nature, and are not proven to work across PVT (process, voltage, temperature) or lack experimental evidence as they are simulation based only. It is therefore reasonable to assume that for commercial products with reasonable yield the maximum frequency of operation is limited by $f_T/4$.

Using this $f_T/4$ metric and the results of Fig. 5 we can draw the following conclusions:

- 10 Gbit/s circuits can be fabricated in the 0.18 $\mu$m CMOS process with $f_T$ of 50 GHz (there are in fact commercial products which accomplish this performance).
- 20 Gbit/s circuits can be fabricated in the 0.13 $\mu$m CMOS process with $f_T$ of 80 GHz (although commercial demand for 20 Gbit/s circuits is not clear).
- Even the 65 nm CMOS process with $f_T$ of 120 GHz might not be fast enough to manufacture 40 Gbit/s circuits. On the other hand advanced SiGe process at 0.18 $\mu$m has $f_T$ of 160 GHz, which should be sufficient for 40 Gbit/s applications.

The simple $f_T/4$ metric can obviously be used only as a basic figure of merit. More detailed considerations are required, in particular for modern CMOS processes which use strained silicon and silicon on insulator (SOI) options.

[5]Typically NRE charges for mask making double from generation to generation.

In fact, one can argue that for analog circuits the maximum frequency of oscillations $f_{max}$[6] is equally important in the determination of the maximum frequency of circuit operation.

Further improvements in MOSFET cutoff and, especially, oscillation frequencies can be achieved using SOI substrates, which increase channel mobility, gate control of the channel and significantly reduce source-bulk and drain-bulk capacitance [22]. The latter two are the dominant capacitive elements in Si MOSFETs at 130 nm and below, and cannot be properly scaled in bulk CMOS processes. Further 30% to 50% improvement in both electron and hole mobilities can be accomplished by using strained Si and SiGe channels on virtual substrate wafers. It is likely that a 90 nm SOI CMOS process incorporating strained silicon channels and reduced parasitic back-end will be adequate for 40 Gbit/s CDR blocks and SERDES ICs operating with full-rate 40 GHz clocks and sub 1.2 V supply.

CMOS scaling down to 90 nm exacerbates several well-known challenges. For digital applications, these include short channel effects, controlling threshold voltage and exponentially increasing leakage currents due to both source/drain and gate currents. For analog circuits additional challenges include IV linearity, low noise characteristics, and transistor matching. To solve these challenges new transistor structures will likely be needed for the 65 nm process generation and below. These include, but are not limited to, ultra-thin body SOI, band-gap engineered transistors (strained Si and SiGe), FinFETs or vertical structures. Only these new structures offer hope of reaching 100 Gbit/s rates in silicon, otherwise InP based devices will have to be used to overcome that speed barrier.

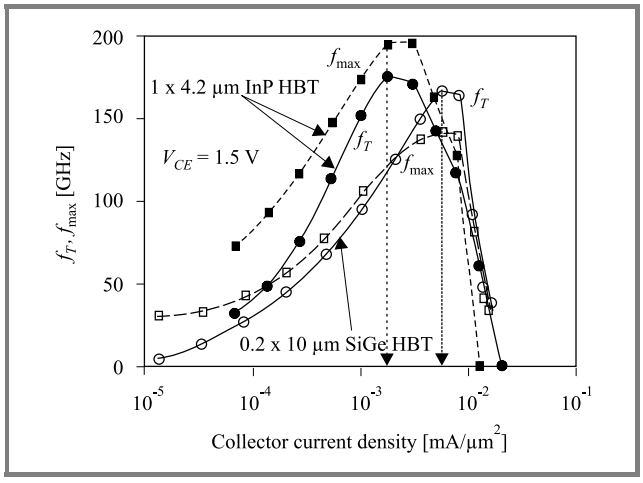


***Fig. 6.*** The cut-off frequency $f_T$ and the maximum oscillation frequency $f_{max}$ for 1 $\mu$m $\times$ 4.2 $\mu$m InP and 0.2 $\mu$m $\times$ 10 $\mu$m SiGe HBTs.

To show the potential behind InP technology Figs. 6 and 7 show the measured $f_T$ and $f_{max}$ data for various high-speed devices. Figure 6 contains the data for 1 $\mu$m $\times$ 4.2 $\mu$m InP and 0.2 $\mu$m $\times$ 10 $\mu$m SiGe HBTs. The InP device achieves higher maximum cut-off frequency of 170 GHz compared to 160 GHz for the SiGe device, and significantly higher maximum oscillation frequency of 200 GHz compared to 130 GHz for the SiGe device.

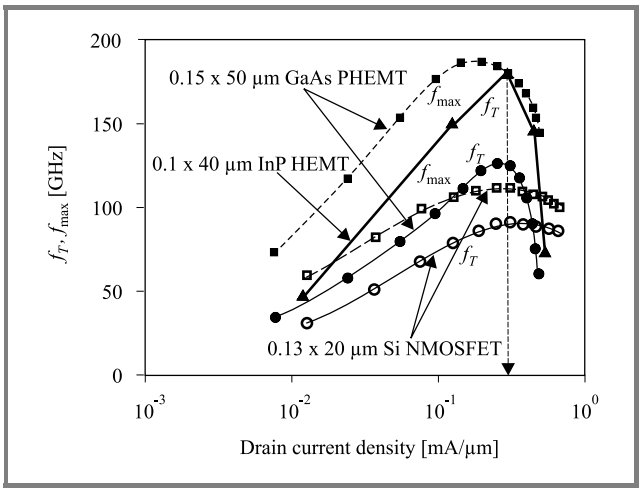


***Fig. 7.*** The cut-off frequency $f_T$ and the maximum oscillation frequency $f_{max}$ 0.13 $\mu$m $\times$ 20 $\mu$m silicon NMOSFET, 0.15$\mu$m $\times$ 50 $\mu$m GaAs PHEMT and 1 $\mu$m $\times$ 4.2 $\mu$m InP HEMT.

Figure 7 contains similar data for 0.13 $\mu$m $\times$ 20 $\mu$m silicon NMOSFET, 0.15 $\mu$m $\times$ 50 $\mu$m GaAs PHEMT[7] and 1 $\mu$m $\times$ 4.2 $\mu$m InP HEMT. Although the slowest among all the devices shown, NMOSFET exhibits a pretty good high-frequency performance with the peak cut-off frequency of over 80 GHz and the maximum frequency of oscillations of 110 GHz. Finally, although not shown in Figs. 6 and 7, it needs to be mentioned that 0.1 $\mu$m InP HEMT device achieves $f_{max}$ of over 300 GHz.

## 5. Design for manufacturability (DFM) of mixed-signal IC's

Intensive scaling down of transistor/wire feature size and supply and signal voltage levels in ICs generates enhanced interest in circuit manufacturability and yield. This has become of particular importance for analog and mixed-signal blocks of CMOS IC systems that are much more sensitive to noise and process variations than digital parts.

The classical yield-optimization approaches developed for digital ICs focus on taking into account the effects of manufacturing defects (lithography defects or spot defects) and manufacturing process variations that result in a spread of electrical performance. Spot defects are quite reliably modeled as spots of extra or missing material, introduced into the process by the inaccuracies of technological operations.

[6]The maximum frequency of oscillations $f_{max}$ is defined as the frequency at which power gain is equal to 1.

[7]HEMT – high electron mobility transistor, a popular high-speed structure for III-V based transistors.

These spot defects can cause shorts or/and breaks in ICs, causing catastrophic defects that degrade IC yield. Possible yield degradation due to spot defects can be evaluated using the critical area approach [23, 24]. This methodology requires adetailed knowledge of defect size distribution in a given technology and circuit layout. Currently, this method finds application in evaluating the potential yield of digital cell libraries offered by different vendors [25].

Estimation of IC yield that takes manufacturing process variations into account should be based on measured process statistics and physical layer (device and circuit level) models that allow statistical modeling of circuit performance versus statistical process variations. This methodology is focused on predicting parametric yield, i.e. the yield resulting from the variation of electrical performance. The Monte-Carlo simulation [26] approach is usually computationally-intensive, which limits its application to circuits containing a relatively small number of MOS transistors. The corner analysis is a simplified way that takes manufacturing process variations into account and includes them sufficiently early in the circuit simulation; it is the one that is practically used throughout the industry.

In digital circuitry spot defects are the major source of catastrophic yield loss. However, the mixed-signal circuits featuring layout with usually larger feature sizes and not as densely packed as digital circuits, are much less affected by spot defects. Instead, they are more prone to parametric faults (and, as a result, parametric yield loss) that originate from such factors as manufacturing process variations, circuit layout (producing various parasitics), or digital noise propagation through the substrate. Consequently, the predictability of the parametric yield of mixed-signal blocks should include a concerted effort totake suspected yield-degrading effects into account as early as possible in the design flow.

It is expected that corner analysis will remain a valuable design tool to estimate the parametric yield of mixed-signal circuits. The validity of this analysis depends to a large extend on the quality of corner models. Most of the corner models used in the industry reflect 3-s (s = standard deviation) changes in the digital circuit performance (usually speed vs. power consumption) due to process variations. These models are also routinely used for evaluating the manufacturability of mixed-signal circuits. How adequate they are for the mixed-signal circuits, remains an open question. New corner models reflecting changes in mixed-signal performance would be more adequate for more accurate parametric yield prediction.

Our experience in mixed-signal CMOS design shows that circuit layout has been one of the major factors contributing to circuit performance and circuit sensitivity [27]. Different layout styles may result in different parasitics and different defect tolerances. Considering different layout solutions requires multiple layout designs, followed by layout extraction and post-layout simulation – a scenario that can not be easily achieved under the time to market pressure. It is believed, however, that this limitation can be mitigated through the automation of layout design of CMOS mixed-signal blocks.

Designing a high quality analog and mixed-signal circuit layout requires usually a human expert and is not a quick procedure. On the other hand, any attempt to automate the process must rely on some degree of layout regularity. But the regularity may be hard to achieve in mixed-signal circuits, where most of the MOS transistors have unique aspect ratios ($W/L$), and many of the transistors must have their I-V characteristics matched. The solution lies in adapting the fully-stacked analog CMOS layout approach [28]. In this technique, MOS transistors are placed in stacks, frequently sharing their sources and drains to minimize parasitic capacitances associated with implanted source/drain regions. Placing MOS transistors in stacks becomes possible due to initial transistor splitting along the channel width, so that a single MOS transistor featuring the channel width, $W$, is implemented as a parallel connection of NMOS transistor segments, each featuring channel width of $W/N$. The fully-stacked CMOS layout technique exploits grouping of MOS transistor segments with similar channel widths into stacks of equal height, that can be later positioned using one of the known placement and routing techniques. The fully-stacked CMOS layout allows also precise MOS transistor matching using common-centroid geometry.

Early attempts [29] to automate mixed-signal CMOS IC layout design aimed at making use of the fully-stacked layout that – by its own nature – minimized drain-substrate and source-substrate p-n junction capacitances. But it is not only the capacitances that need to be minimized. A very compact fully-stacked layout usually requires a more complex metal interconnection pattern. Since metal interconnects constitute another source of parasitic capacitances, the challenge is in making an intelligent tradeoff between the compactness of the fully-stacked layout and the number and lengths of metal interconnects, which is a tradeoff between p-n junction capacitances, and metal wire-to-substrate capacitances. The new methodology [30] proposes to use an automated layout design tool to generate multiple layouts of the same circuit, followed by a post-layout extraction and circuit simulation to evaluate circuit performance, and to choose the most effective layout solution. The same approach can be coupled in future with the manufacturability analysis of mixed-signal CMOS ICs.

As mixed-signal circuits grow in complexity, the need for development of behaviour-level models of mixed-signal blocks rises dramatically. These models can aid in efficient mixed-signal system design through proper system partitioning and mixing behaviour-level and circuit-level simulation within the same CAD tool. Behavioural models can be customized to allow statistical simulation, as well as noise modeling. However, technology-specific system implementations do require substantial model building and model characterization activity to fully utilize potential benefits that come from the use of behaviour-level design for manufacturability.

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