Paper

A 24 GHz PHEMT-based oscillator

Arkadiusz Lewandowski, Günter Kompa, Wilfred Mwema, and Wojciech Wiatr

Abstract — We present a systematic nonlinear procedure for designing microwave oscillators utilising a nonlinear PHEMT model, the negative resistance approach and the describing function concept. The procedure is applied in the design of a 24 GHz oscillator, which is then realised in hybrid technology. Measurement results show −6% shift in the frequency but an acceptable agreement in the output power. A detailed analysis shows that the frequency shift arises mainly from inadequate CAD models in the *K* band, for the microstrip components employed in our design.

Keywords — microwave oscillator, oscillator design method, negative resistance, describing function, nonlinear PHEMT model, microstrip components models.

1. Introduction

The rapid growth of MMIC market calls for a continuous improvement in design techniques to facilitate a fast and inexpensive realisation of new circuits. While oscillators play a leading role in every radio communication system, their design at high operating frequencies is particularly difficult, mainly due to nonlinear properties of the active device. This implies that the nonlinear properties have to be not only correctly represented with an adequate transistor model [1], but also properly accounted for during circuit analysis and optimization. The complexity of these tasks is such that a simplified approach is often required to attain a reasonable solution effectively.

Various oscillator design approaches for microwave applications have been proposed. However there is still no clear optimal lane to follow. Simple design methods, based on small-signal scattering parameter description [2–4], allow estimating the oscillation frequency, but they fail in the prediction of the oscillator output power. Thus, experimental tuning is often needed. Moreover, thorough studies have recently shown that these methods may even lead to false judgments [5–7].

Superior results may be obtained using methods that combine small-signal analysis with some elements of nonlinear approach based on an analysis of the DC-characteristics of the active device [8]. However, the most accurate designs must involve large-signal design procedures that employ the harmonic balance method and optimization techniques implemented in majority of modern professional CAD programs [4, 9, 10]. Unfortunately, the use of these methods is not as easy as their simpler counterparts due to the problem of local minima arising during the optimization [10].

The aim of the work reported in this paper, was to develope a simplified, yet consistent nonlinear design procedure that improves the prediction of the output power and oscillation frequency in *K*-band GaAs FET-based oscillators. The procedure was developed on the basis of a wide review of various existing methods and applied in the design of a 24 GHz oscillator [7]. Measurement results for the oscillator realized will be presented and discussed.

2. Large-signal PHEMT model

For the design, a PHEMT chip transistor AFP02N3 from Alpha Industries was selected and a simplified large-signal model, based on the topology shown in Fig. 1, developed. In this model, the parasitic effects, related to the metalisation pattern, contact pads and bonding wires, are represented by capacitances C_{pgi}, C_{pdi}, C_{pga}, C_{pda} and inductances L_g, L_s, L_d. The only nonlinear elements are the controlled current source i_{DS} and the capacitance C_{gs}. The current source i_{DS} is described through formulae taken directly from the Chalmers FET model [11]. Unfortunately, this model describes both capacitances C_{gd} and C_{gs} using nonlinear formulae that do not meet simple physical rules [1]. To circumvent this problem, C_{gd} has been treated as linear and C_{gs} represented by a simplified relationship [12], valid in the i_{DS} saturation region.

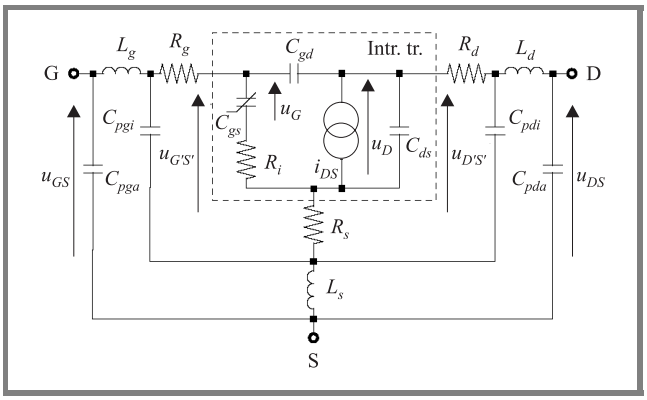


Fig. 1. Topology of large-signal PHEMT model.

The values of the equivalent circuit's elements were extracted from multi-bias small-signal S-parameter measurements of the transistor using the method presented in [13, 14]. The parameters of the function $C_{gs}(u_G)$ were then determined using a least-squares optimization. The results of the fit are shown in Fig. 2.

Using another least-squares optimization, the i_{DS} model parameters were extracted from the measured DC transistor characteristics. The fit obtained is shown in Fig. 3,

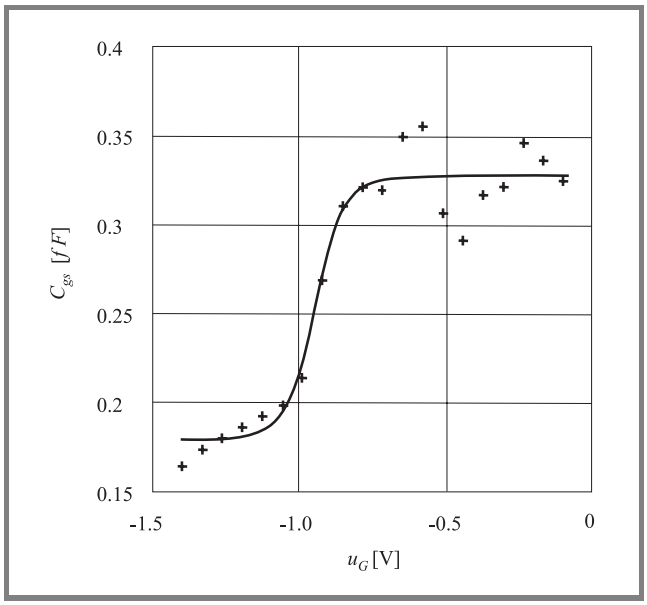


Fig. 2. Dependence of C_{gs} on u_G: measured (+) and fitted (-).

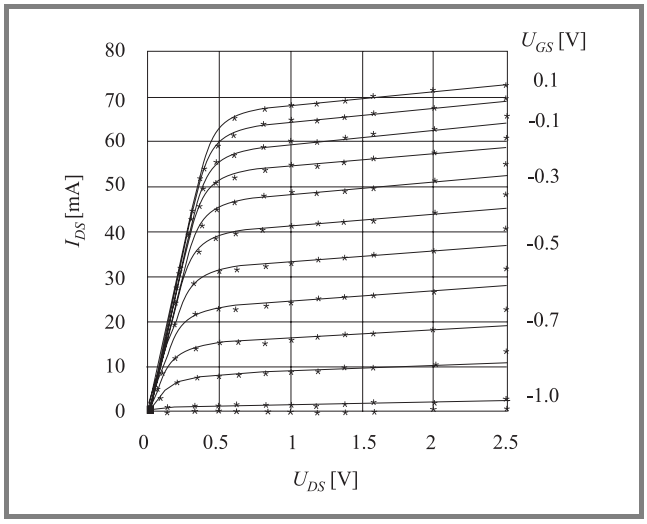


Fig. 3. PHEMT output characteristics: measured (x) and fitted (-).

which is in good agreement with the measurement for $U_{DS} < 2.0$ V. To avoid PHEMT operation in the ohmic region and soft-breakdown effects, not accounted for by the Chalmers model, the analyses were confined in the region bounded by $1.0\text{ V} < U_{DS} < 2.0\text{ V}$ and $-1\text{ V} < U_{GS} < 0.1\text{ V}$. Note that this model neglects the dispersion effects often noticed in microwave FETs [1]. This model was then employed in the oscillator design.

3. Oscillator design

A general oscillator configuration is shown in Fig. 4. The circuit can be split into an active and a load network along the dotted line as shown in this figure. The active network consists of the active device A with the feedback reactances jX_1 and jX_2. The load network is formed by a matching network MN, presumably lossless, terminated with $Z_0 = 50\ \Omega$. This circuit division corresponds with two relevant design steps.

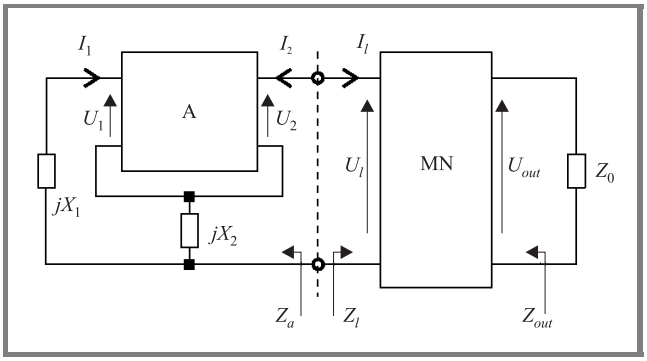


Fig. 4. General oscillator configuration.

3.1. Optimization of the active network

In this step, the optimal large-signal operating conditions and feedback reactances of the active network are sought for maximum power transfer and low harmonic content. To provide a good starting point for this optimization, we first evaluate the currents and voltages of the intrinsic transistor using the technique of Abe [8] based on the maximization of the power delivered by the active device, i.e. added power $P_{add} = -1/2\,\mathrm{Re}\,[U_1 I_1^* + U_2 I_2^*]$. To this end, the amplitudes U_g and U_d and their phase difference are adjusted keeping the intrinsic load cycle within the limits of the saturation region in the DC-characteristics specified earlier. These calculations utilise the small-signal transistor parameters and a linear analysis. Having determined U_1 and U_2, initial values for the reactances X_1 and X_2 are calculated using simple formula [8].

A large-signal optimization of the active device is then performed using the approach proposed by Andre *et. al.* [10]. An independent voltage source operating at a given frequency f_0 is attached to the network and the power dissipated in this source maximized through the harmonic balance method and a gradient optimization technique. Simultaneously, the harmonic content in the current is kept sufficiently low. In this way, the optimal voltage U_l^{opt} and current I_l^{opt} are determined and the reactances X_1 and X_2 are modified. Contrary to the technique in [10], no particular shape of the intrinsic load cycle is assumed during the optimization since this may lead to suboptimal results [7].

3.2. Design of the load network

This design aims at terminating the active network with the optimal impedance $Z_l^{opt} = U_l^{opt}/I_l^{opt}$ such that it operates at the steady-state voltage U_l^{opt} and current I_l^{opt} determined in the previous step. This goal is attained iteratively.

In the first step, the matching network MN, capable of transforming the standard matched load Z_0 into Z_l^{opt}, is defined. The oscillation start-up and build-up conditions and the equilibrium-state stability are then verified. The matching network and eventually the active one are continuously modified until all the conditions are met.

In verifying the fundamental oscillation start-up conditions at a frequency f_0', following general immitance terms are utilised:

$$\mathrm{Re}\,[W_{out}(f_0') + W_0] > 0; \quad \mathrm{Im}\,[W_{out}(f_0') + W_0] = 0, \qquad (1)$$

where W stands for immitance and indices *out* or 0 refer to the MN output or the matched load, respectively (see Fig. 4). Both the impedance and admittance forms of (1), corresponding with the relevant series or parallel resonant circuit representation, are considered. Only one of the two forms at a single frequency f_0', lying close enough to the required oscillator's frequency f_0, should be satisfied, to preclude any parasitic oscillation in the circuit.

The verification of the oscillations build-up conditions and the equilibrium-state stability is based on a describing function (DF) [15], which is the large-signal impedance Z_{out} for the fundamental Fourier component. The first verification lends itself to checking whether the inequality in (1) is satisfied for amplitudes $|U_{out}| < |U_{out}^{opt}|$, where U_{out}^{opt} corresponds with U_l^{opt}. As shown in Fig. 5, this inequality is satisfied for all intermediate states Q_0, Q_1 and Q_2 hence oscillations may build up from the initial state till the equilibrium state P. The oscillation frequency for each state is defined by Eq. (1) and marked on Fig. 5.

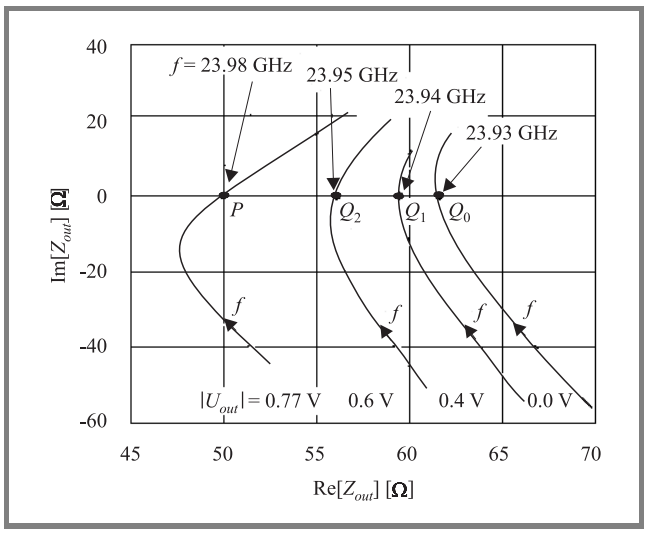


Fig. 5. Dependence of Z_{out} on frequency f for $|U_{out}| = \text{const}$.

In the steady-state, the stability of the oscillations, with regard to their frequency f and amplitude U_{out}, is examined. This involves checking a simple inequality, based on the DF, which is analogous to the well-known Kurokawa's stability condition [16].

4. Circuit realization

The oscillator was realised in hybrid technology using a 375 μm thick teflon laminate. The layout of the oscillator is shown in Fig. 6. The PHEMT chip is placed in the middle of the board marked and bonded using a 25 μm gold wire. The pair of identical shorted source stubs of a length greater than $\lambda/4$ constitutes a source capacitance, while the gate subcircuit acts as an inductance. The later comprises an open $\lambda/4$ stub, a main gate stub and a bias network. The drain subcircuit consists of a bias network, a matching network comprising a transmission line and an open stub, and a coupling capacitor to the output composed of two coupled $\lambda/4$ lines.

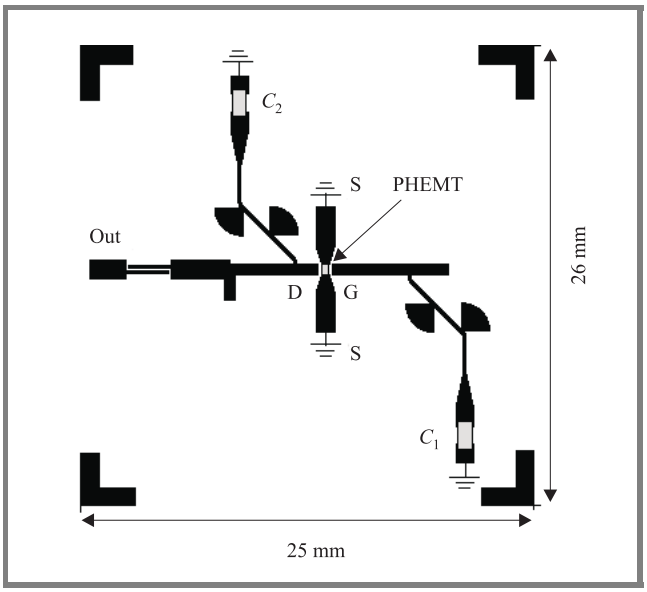


Fig. 6. The oscillator layout.

Two different PHEMT chips were successively bonded on the same PCB thus offering an opportunity to examine the effect of device variation. Both PHEMT chips exhibited a shift in their pinch-off voltage relative to the data sheet specification and their U_{GS} required individual correction, in order to obtain the design bias point $I_{DS} = 33$ mA and $U_{DS} = 1.6$ V. The output power was then measured and found to be in good agreement with the predicted value. However, the oscillation frequency was approximately 6% lower than the design frequency.

To study this problem more thoroughly, oscillator tuning characteristic versus U_{GS} was measured and depicted in Fig. 7 for both oscillator versions. The frequency shift may be attributed to the passive network, since only its slight dependence on U_{GS} can be noticed. Moreover, Fig. 7 reveals significant differences in the output power and efficiency traces obtained for each oscillator version. This may be caused partly by the nonrepeatability of the

bonding connections and partly by the variation in transistor characteristics across devices of the same type.

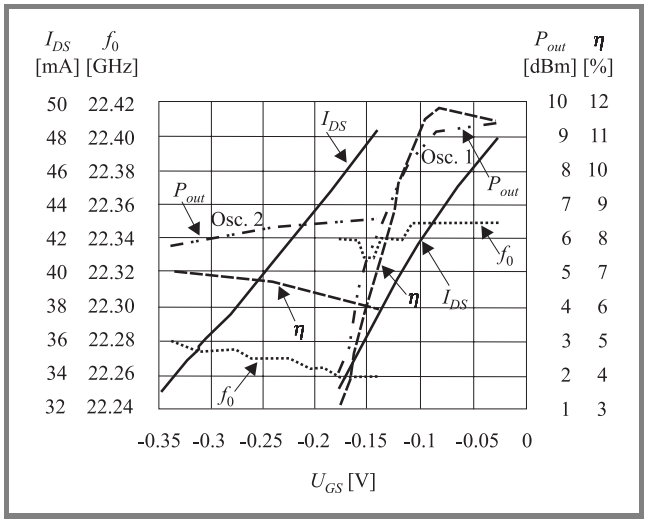


Fig. 7. Measurement results.

To check the above hypotheses, electromagnetic (EM) simulations of the layout and a sensitivity analysis of the oscillator circuit were performed. The EM simulations showed that the main contribution to the frequency shift comes from inadequacy of microstrip components models, we used for the designing, in the *K* band [17]. Moreover, a high sensitivity of the output resistance R_{out} and consequently the output power to the variation of the transconductance g_m and the source reactance was found. The analyses proved strong effects of the gate and source stub lengths, and bonding inductances on both the power and frequency.

5. Conclusions

A consistent nonlinear design procedure for microwave oscillators has been developed, utilising the Chalmers nonlinear HEMT model, the negative resistance approach and the describing function concept. The procedure has been applied in the design and realization of a 24 GHz PHEMT-based oscillator in hybrid technology. Measurements showed -6% shift in the frequency but an acceptable agreement in the predicted signal power. Further EM simulation of the oscillator layout explained this shift as mainly coming from inadequate CAD models of microstrip components used in the design. Sensitivity analysis performed on the circuit revealed the need for a more repeatable interconnect technology than wire bonding, e.g. flip-chip or quasi-monolitic [18] technology, for successful realization of such oscillators. This analysis emphasises the relevance of reliable CAD models of passive components for accurate nonlinear oscillator design, particularly at milimeter waves.

References

[1] I. Schmale, "Entwicklung eines konsistenten elektrothermischen Grosssignalmodells für Feldeffekttransistoren als Grundlage für den zuverlässigen Entwurf monolitischer Frequenzverdoppler". Ph.D. thesis, Univeristät Gesamthochschule Kassel, Kassel, 1999.

[2] E. Wasige, H. J. de la Torre, I. Ak-Layla, and G. Kompa, "An analytical design procedure for microwave oscillators based on S-parameters", in *Int. IEEE Worksh. Experim. Bas. FET Dev. Model. Relat. Nonlin. Circ. Des.*, Universität Gesamthochschule Kassel, Kassel, 1997, pp. 41.1–41.3.

[3] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*. Englewood Cliffs, NJ: Prentice-Hall, 1997.

[4] R. Howald, "A 24 GHz HEMT microstrip oscillator using linear and nonlinear CAD techniques", *Microw. J.*, pp. 80–93, May 1994.

[5] S. Savaria and P. Champagne, "Linear simulators for use in oscillator design", *Microw. J.*, pp. 98–105, May 1995.

[6] M. Odyniec, "Oscillator stability analysis", *Microw. J.*, pp. 66–76, June 1999.

[7] A. Lewandowski, "Generator sygnału sinusoidalnego 24 GHz". Praca magisterska, Wydział Elektroniki i Technik Informacyjnych, Politechnika Warszawska, Warszawa, 2001 (M.Sc. thesis in Polish).

[8] H. Abe, "A GaAs MESFET oscillator quasi-linear design method", *IEEE Trans. Microw. Theory Techn.*, vol. MTT-34, pp. 19–25, 1986.

[9] A. V. Grebennikov, "Microwave transistor oscillators: an analytic approach to simplify computer-aided design", *Microw. J.*, pp. 292–300, May 1999.

[10] P. André, J. Dienot *et al.*, "Microwave oscillator design from load cycle optimisation – application to MMIC GaAs MESFET oscillator", in *Proc. 24th EuMC*, 1994, pp. 831–835.

[11] I. Angelov, H. Zirath, and N. Rorsman, "A new empirical model for HEMT and MESFET devices", *IEEE Trans. Microw. Theory Techn.*, vol. MTT-40, pp. 2258–2266, 1992.

[12] U. Schaper and A. Werthof, "Large-signal HEMT model for resitive mixer design", in *Int. IEEE Worksh. Experim. Bas. FET Dev. Model. Relat. Nonlin. Circ. Des.*, Universität Gesamthochschule Kassel, Kassel, 1997, pp. 26.1–26.5.

[13] F. Lin and G. Kompa, "FET model parameter extraction based on optimization with multiplane data-fitting and bidirectional search – a new concept", *IEEE Trans. Microw. Theory Techn.*, vol. MTT-42, pp. 1114–1120, 1994.

[14] W. Mwema and G. Kompa, "A new simplified and reliable HEMT modelling approach using pinched cold FET S-parameters", in *Proc. MTTS 2000*.

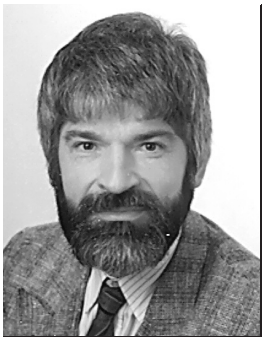
[15] A. Gelb and W. Vander Velde, *Multiple-Input Describing Functions and Nonlinear System Design*. New York: McGraw-Hill Book Company, 1968.

[16] K. Kurokawa, "Some basic characteristics of broadband negative resistance oscillator circuits", *Bell Syst. Tech. J.*, pp. 1937–1955, July-Aug. 1969.

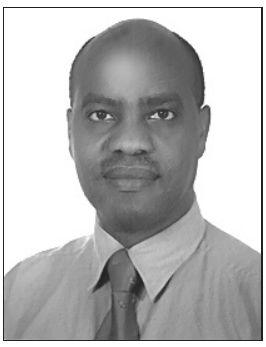
[17] A. Lewandowski and W. Wiatr, "Verification of CAD models for microstrip components using FD-TD method", in *Proc. 14th Microw. Conf. MIKON-2002*, Gdańsk, Poland, May 2002, pp. 357–360.

[18] E. Wasige, G. Kompa, F. van Raay, W. Scholz, I. Rangelow, F. Shi, R. Kassing, R. Meyer, and M.-C. Amann, "A new technological concept for optimum circuit design at microwave and milimeter-wave frequencies", in *Int. IEEE Worksh. Experim. Bas. FET Dev. Model. Relat. Nonlin. Circ. Des.*, Universität Gesamthochschule Kassel, Kassel, 1997, pp. 23.1–23.5.

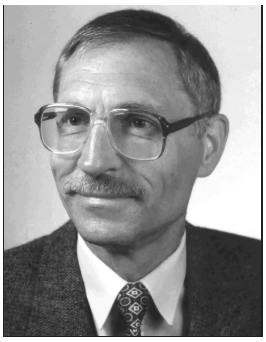
Arkadiusz Lewandowski received the M.Sc. degree in electronic engineering from Warsaw University of Technology, Poland, in 2001. Currently he is working towards Ph.D. degree at the Institute of Electronic Systems, Warsaw University of Technology. His main research interests include oscillator design and simulation methods, modelling of active microwave devices and microwave on-wafer measurements.
e-mail: A.Lewandowski@elka.pw.edu.pl
Institute of Electronic Systems
Warsaw University of Technology
Nowowiejska st 15/19
00-665 Warsaw, Poland



Günter Kompa was awarded the Dipl.-Ing. and the Dr.-Ing. degrees from the R.W.T.H., Aachen, Germany in 1970 and 1975, respectively. He joined Endress & Hauser, Germany in 1976 focusing on microwave and laser radar research and development. He won the 1978 Heinrich-Hertz Award from Institute of Radio and Electronic Engineers, London. Since 1984, he has been a Professor heading the Department of Microwave Technology at the University of Kassel, Germany. He is referee for the German Ministry of Research and Technology (BMBF) and the German Academic Exchange Service (DAAD) since 1990 and 1997, respectively. He established the masters course "Electrical Communication Engineering" at the University of Kassel, which is one of the first and only eight international postgraduate degree courses in Germany. His current research interests cover mainly circuit and system design of UWB microwave and laser radar, characterization and modelling of high power amplifiers both at device and system levels, and amplifier linearization algorithms. He has published over 150 technical papers and filed numerous patents.
e-mail: kompa@hfm.e-technik.uni-kassel.de
Fachgebiet Hochfrequenztechnik
University of Kassel
Wilhelmshöher Allee 73
D-34121 Kassel, Germany



Wilfred Mwema obtained the B.T. degree in electrical and communication technology from Moi University and M.Sc. in electrical engineering from the University of Nairobi, Kenya, respectively. Since October 1997, has been pursuing Ph.D. degree in electrical engineering at the University of Kassel, Germany, where he has been working on microwave characterisation and modelling of GaAs-based field-effect transistors and just successfully completed his studies. His interests include microwave oscillator design, among other topics.
e-mail: mwema@hfm.e-technik.uni-kassel.de
Fachgebiet Hochfrequenztechnik
University of Kassel
Wilhelmshöher Allee 73
D-34121 Kassel, Germany



Wojciech Wiatr received the M.Sc., and Ph.D. degrees in electronic engineering from Warsaw University of Technology, Warsaw, Poland in 1970 and 1980, respectively. For 30 years he has been with the Institute of Electronic Systems at the Warsaw University of Technology. His main scientific interests are in the field of precision microwave measurements. He has been developing new techniques and instrumentation for broadband scattering and noise parameter measurements of microwave transistors and MMICs. He invented the RF multi-state total power radiometer for simultaneous noise and vector analysis of microwave networks using natural noise excitation. Dr. Wojciech Wiatr published 1 book, over 80 papers and holds two patents.
e-mail: Wiatr@ise.pw.edu.pl
Institute of Electronic Systems
Warsaw University of Technology
Nowowiejska st 15/19
00-665 Warsaw, Poland